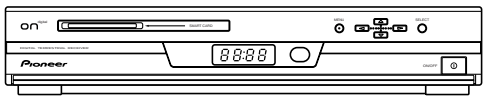
Service Manual



ORDER NO.
ARP3088

DIGITAL TERRESTRIAL RECEIVER

DBR-T210GBS

DIGITAL TERRESTRIAL RECEIVER (PRE-PAID BOX)

DBR-T210GBP

DIGITAL TERRESTRIAL RECEIVER (PRE-PAID PLUS)

DBR-T210GBN

THIS MANUAL IS APPLICABLE TO THE FOLLOWING MODEL(S) AND TYPE(S).

Type	Model			Power Requirement	Remarks
	DBR-T210GBS	DBR-T210GBN	DBR-T210GBP		
NVXK	◯	◯	◯	AC230V	

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PIONEER CORPORATION 4-1, Meguro 1-chome, Meguro-ku, Tokyo 153-8654, Japan
PIONEER ELECTRONICS SERVICE, INC. P.O. Box 1760, Long Beach, CA 90801-1760, U.S.A.
PIONEER EUROPE NV Haven 1087, Keetberglaan 1, 9120 Melsele, Belgium
PIONEER ELECTRONICS ASIACENTRE PTE. LTD. 253 Alexandra Road, #04-01, Singapore 159936

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1. SAFETY INFORMATION

This service manual is intended for qualified service technicians ; it is not meant for the casual do-it-yourselfer. Qualified technicians have the necessary test equipment and tools, and have been trained to properly and safely repair complex products such as those covered by this manual.
Improperly performed repairs can adversely affect the safety and reliability of the product and may void the warranty. If you are not qualified to perform the repair of this product properly and safely, you should not risk trying to do so and refer the repair to a qualified service technician.

WARNING
This product contains lead in solder and certain electrical parts contain chemicals which are known to the state of California to cause cancer, birth defects or other reproductive harm.

Health & Safety Code Section 25249.6 – Proposition 65

NOTICE
(FOR CANADIAN MODEL ONLY)
Fuse symbols (fast operating fuse) and/or (slow operating fuse) on PCB indicate that replacement parts must be of identical designation.

REMARQUE
(POUR MODÈLE CANADIEN SEULEMENT)
Les symboles de fusible (fusible de type rapide) et/ou (fusible de type lent) sur CCI indiquent que les pièces de remplacement doivent avoir la même désignation.

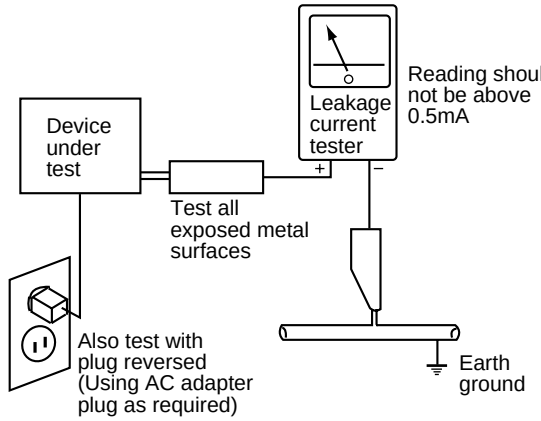
(FOR USA MODEL ONLY)

1. SAFETY PRECAUTIONS

The following check should be performed for the continued protection of the customer and service technician.

LEAKAGE CURRENT CHECK

Measure leakage current to a known earth ground (water pipe, conduit, etc.) by connecting a leakage current tester such as Simpson Model 229-2 or equivalent between the earth ground and all exposed metal parts of the appliance (input/output terminals, screwheads, metal overlays, control shaft, etc.). Plug the AC line cord of the appliance directly into a 120V AC 60Hz outlet and turn the AC power switch on. Any current measured must not exceed 0.5mA.


Reading should not be above 0.5mA
Leakage current tester
+
–
Device under test
Test all exposed metal surfaces
Also test with plug reversed (Using AC adapter plug as required)
Earth ground

AC Leakage Test

ANY MEASUREMENTS NOT WITHIN THE LIMITS OUTLINED ABOVE ARE INDICATIVE OF A POTENTIAL SHOCK HAZARD AND MUST BE CORRECTED BEFORE RETURNING THE APPLIANCE TO THE CUSTOMER.

2. PRODUCT SAFETY NOTICE

Many electrical and mechanical parts in the appliance have special safety related characteristics. These are often not evident from visual inspection nor the protection afforded by them necessarily can be obtained by using replacement components rated for voltage, wattage, etc. Replacement parts which have these special safety characteristics are identified in this Service Manual.

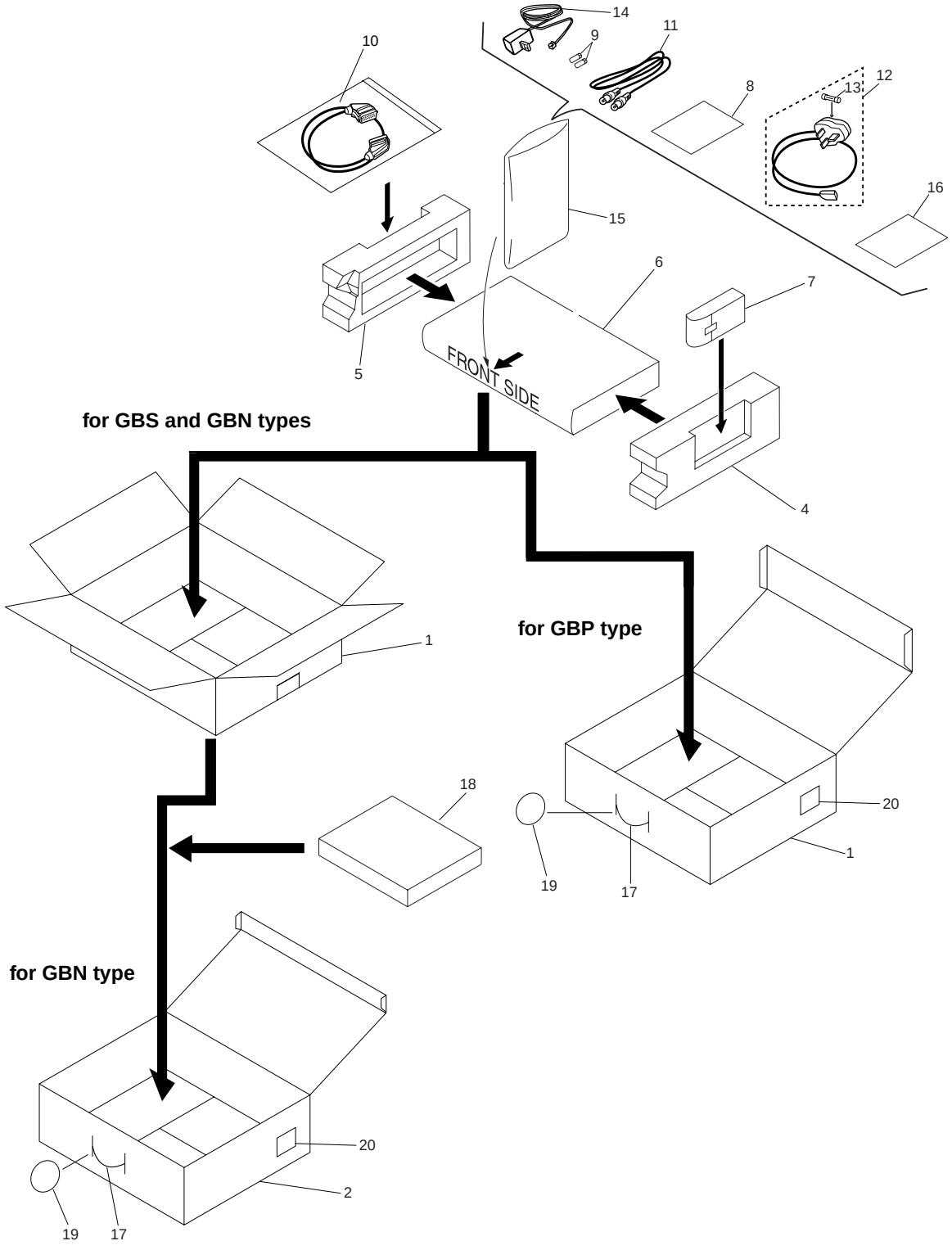
Electrical components having such features are identified by marking with a ⚠ on the schematics and on the parts list in this Service Manual.
The use of a substitute replacement component which does not have the same safety characteristics as the PIONEER recommended replacement one, shown in the parts list in this Service Manual, may create shock, fire, or other hazards.

Product Safety is continuously under review and new instructions are issued from time to time. For the latest information, always consult the current PIONEER Service Manual. A subscription to, or additional copies of, PIONEER Service Manual may be obtained at a nominal charge from PIONEER.

2. EXPLODED VIEWS AND PARTS LIST

NOTES: ●*Parts marked by "NSP" are generally unavailable because they are not in our Master Spare Parts List.*
●*The ⚠ mark found on some component parts indicates the importance of the safety factor of the part. Therefore, when replacing, be sure to use parts of identical designation.*
●*Screws adjacent to ▼ mark on the product are used for disassembly.*

2.1 PACKING



(1) PACKING PARTS LIST

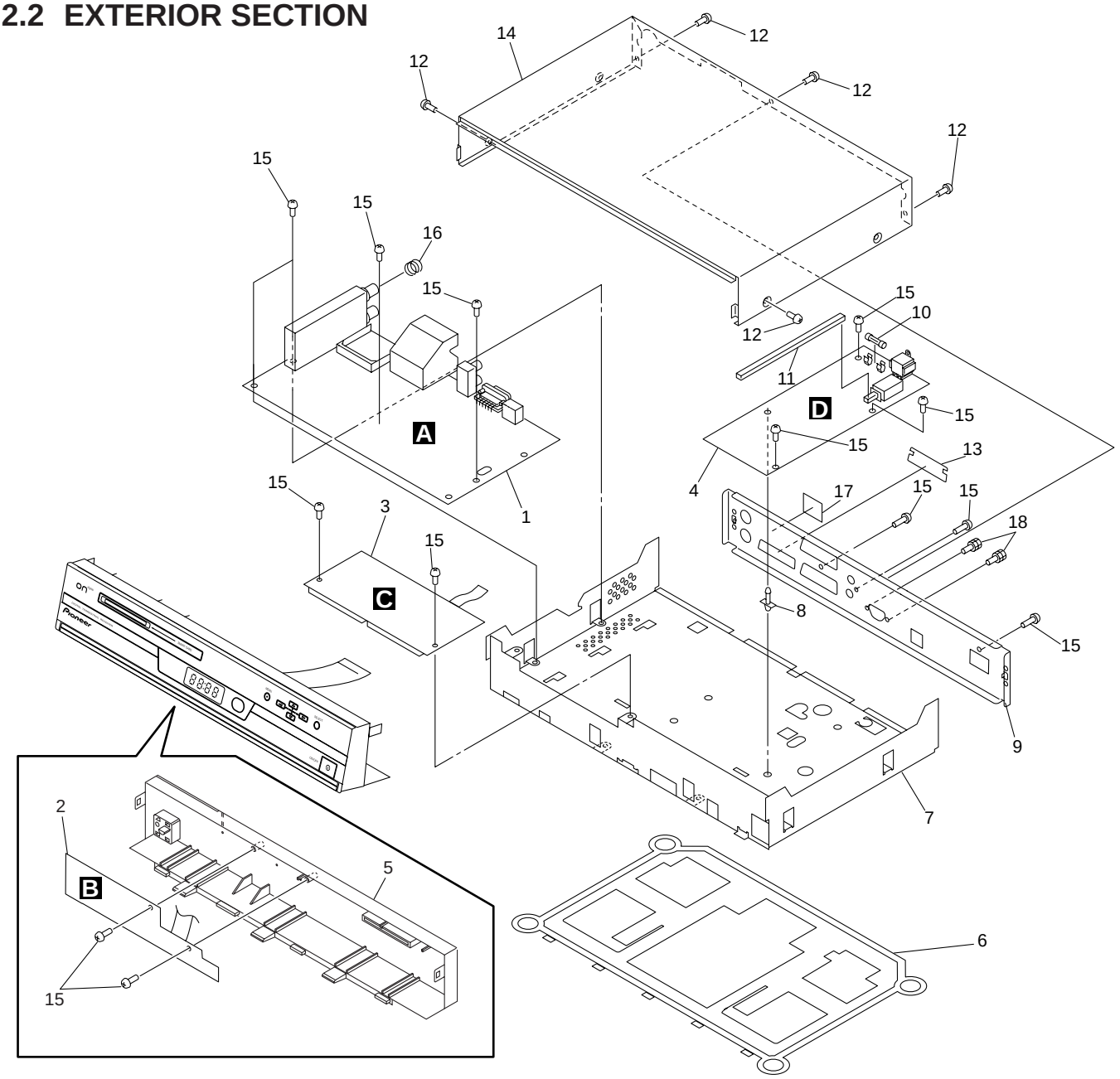
Mark	No.	Description	Part No.
	1	PACKING CASE	See Contrast table (2)
	2	MASTER CARTON	See Contrast table (2)
	3	• • • • • • • • • • • • • •	
	4	SIDE PAD R	BHA1147
	5	SIDE PAD L	BHA1146
	6	SHEET	AHG1153
	7	REMOTE CONTROL UNIT	BXD1040
	8	INSTRUCTION BOOK (English)	XRB1013
NSP	9	BATTERY (R6) 2P	VEM1017
	10	SCART LEAD (1.5m:Black)	XDH1001
	11	AERIAL/RF LEAD	BDE1064
⚠	12	MAINS LEAD(2m:Black)	ADG7009
⚠	13	FUSE (T5A)	AEK7001
	14	TELEPHONE MODEM CABLE (10m:White)	BDH1024
NSP	15	CATALOGUE BAG	BHG1047
NSP	16	CA CARD KIT	See Contrast table (2)
	17	HANDLE	See Contrast table (2)
	18	NET BOX	See Contrast table (2)
NSP	19	PACKING SEAL	See Contrast table (2)
NSP	20	EAN CODE LABEL	See Contrast table (2)

(2) CONTRAST TABLE

DBR-T210GBS, DBR-T210GBP and DBR-T210GBN are constructed the same except for the following:

Mark	No.	Symbol and Description	Part No.			Remarks
			DBR-T210GBS	DBR-T210GBP	DBR-T210GBN	
	1	PACKING CASE	XHD1021	BHD1497	XHD1021	
	2	MASTER CARTON	Not used	Not used	BHD1499	
NSP	16	CA CARD KIT	BPK1021	BPK1025	BPK1026	
	17	HANDLE	Not used	BEC1242	BEC1242	
NSP	18	NET BOX	Not used	Not used	BXD1051	
NSP	19	PACKING SEAL	Not used	BAX1291	BAX1291	
NSP	20	EAN CODE LABEL	Not used	XAX1001	XAX1002	

2.2 EXTERIOR SECTION



(1) EXTERIOR PARTS LIST

Mark	No.	Description	Part No.
	1	MAIN ASSY	XWE1003
	2	FRONT ASSY	XWE1004
	3	CARD ASSY	XWE1006
⚠	4	POWER ASSY	XXF1002
	5	FRONT PANEL ASSY	BWX1194
	6	PLASTIC BASE(PLS)	BMA1002
	7	CHASSIS(MET)	BNA1151
	8	PCB SUPPORT	AEC1215
	9	REAR PANEL ASSY	XWX1004
⚠	10	FUSE (F101 : T2.5AH250V)	REK1102
	11	JOINT	BMR1133
	12	SCREW	BBZ30P080FNI
	13	REAR PANEL COVER	BAP1003
	14	BONNET CASE(MET)	BNE1129
	15	SCREW	BBZ30P080FZK
	16	EARTH SPRING	XBH1003
NSP	17	NAME LABEL	See Contrast table (2)
	18	HEXAGON HEAD SCREW	BBA1059

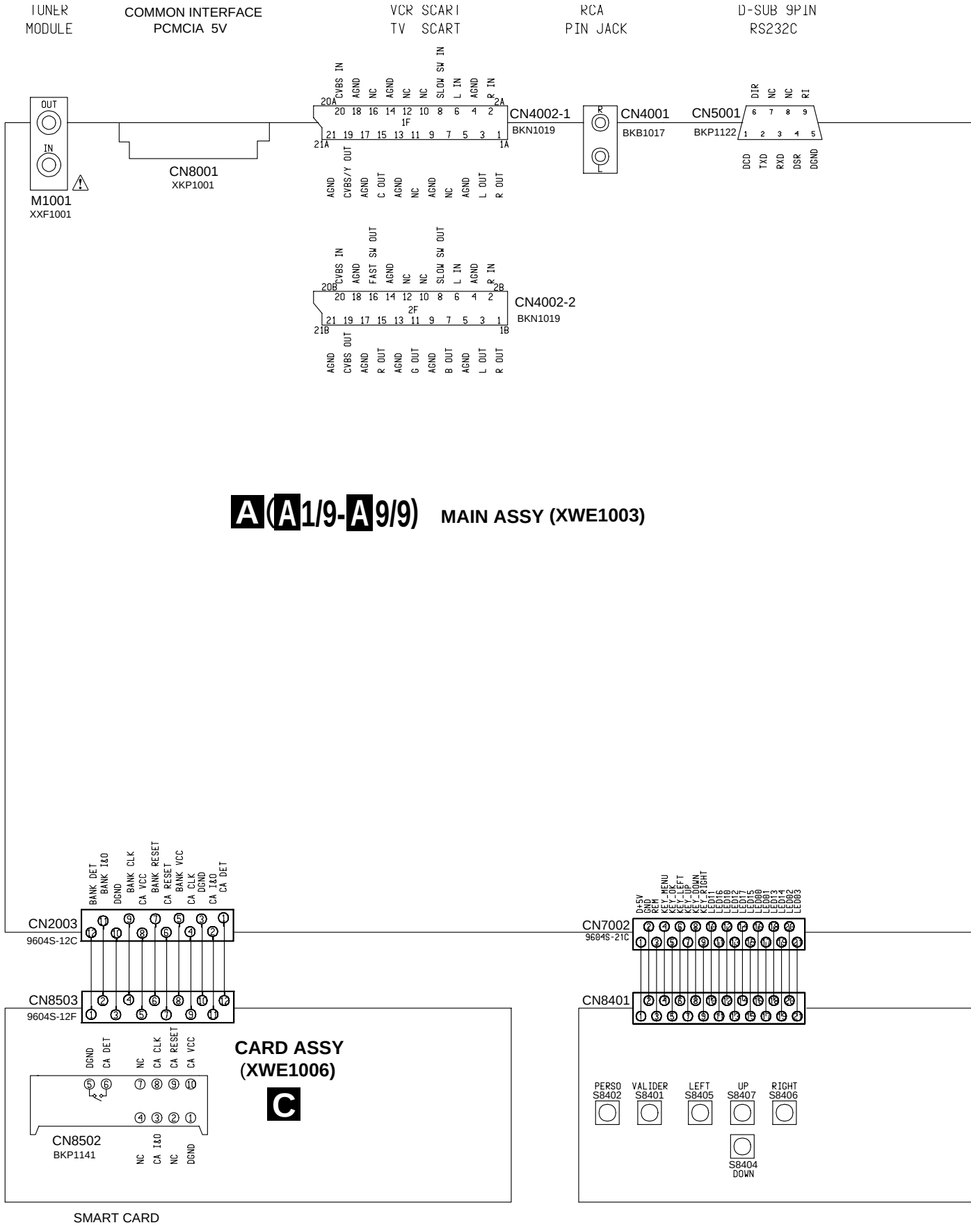
(2) CONTRAST TABLE

DBR-T210GBS, DBR-T210GBP and DBR-T210GBN are constructed the same except for the following:

Mark	No.	Symbol and Description	Part No.			Remarks
			DBR-T210GBS	DBR-T210GBP	DBR-T210GBN	
NSP	17	NAME LABEL	XAL1006	XAL1007	XAL1008	

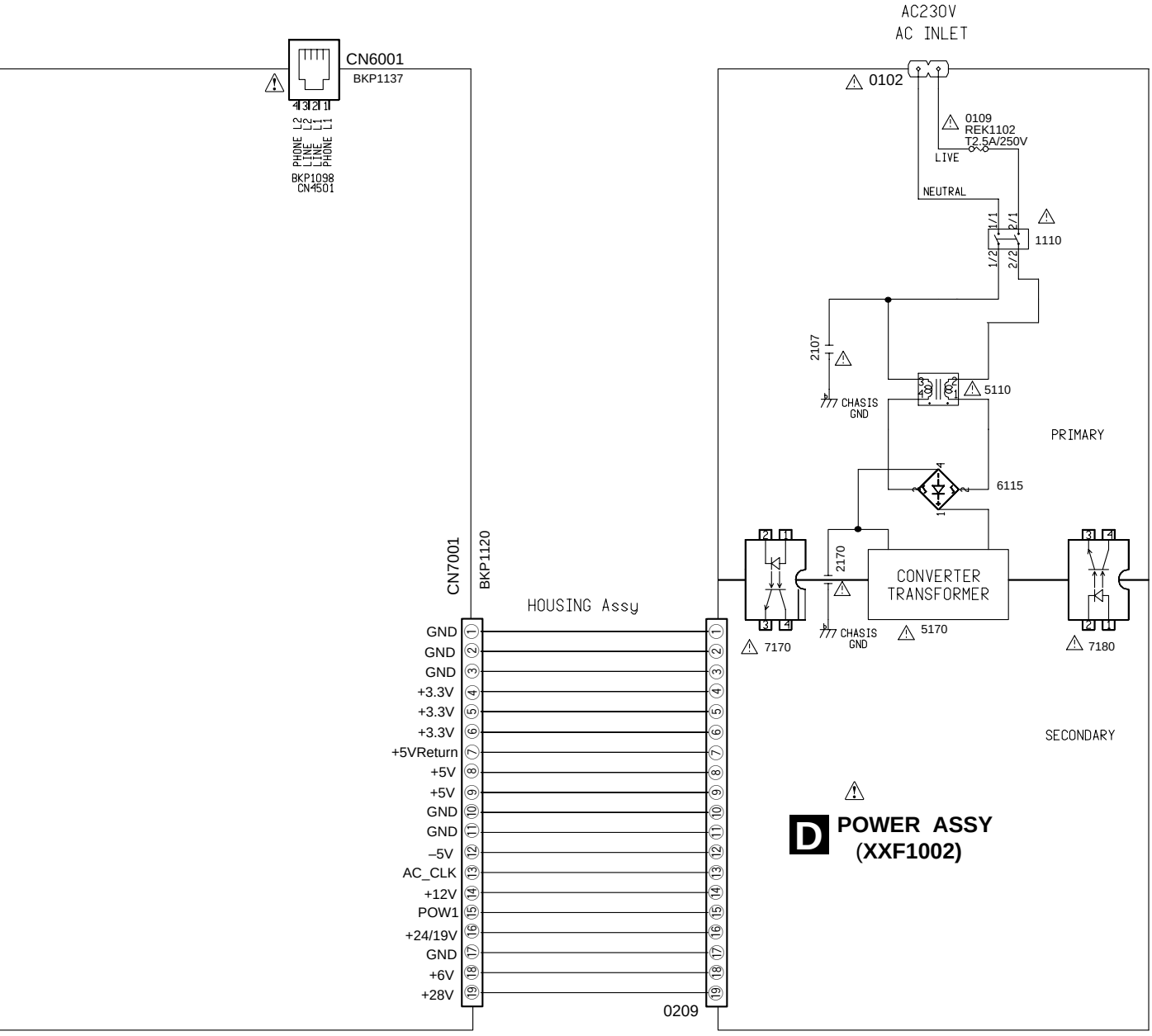
3. SCHEMATIC DIAGRAM

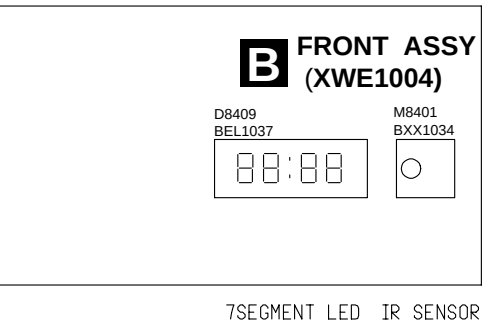
3.1 OVERALL WIRING DIAGRAM


TUNER MODULE
COMMON INTERFACE PCMCIA 5V
VCR SCART TV SCART
RCA PIN JACK
D-SUB 9PIN RS232C
OUT
IN
M1001
XXF1001
CN8001
XKP1001
CVBS IN AGND NC AGND NC NC SLOW SW IN L IN AGND R IN
20A 20 18 16 14 12 10 8 6 4 2 2A
1F
21A 21 19 17 15 13 11 9 7 5 3 1 1A
CN4002-1
BKN1019
AGND CVBS/Y OUT AGND C OUT AGND NC AGND NC AGND L OUT R OUT
CN4001
BKB1017
CN5001
BKP1122
DIR NC NC RI
6 7 8 9
1 2 3 4 5
DCD TXD RXD DSR DGND
CVBS IN AGND FAST SW OUT AGND NC NC SLOW SW OUT L IN AGND R IN
20B 20 18 16 14 12 10 8 6 4 2 2B
2F
21B 21 19 17 15 13 11 9 7 5 3 1 1B
CN4002-2
BKN1019
AGND CVBS OUT AGND R OUT AGND G OUT AGND B OUT AGND L OUT R OUT
A(A1/9-A9/9) MAIN ASSY (XWE1003)
BANK DET BANK I&O DGND BANK CLK CA VCC BANK RESET CA RESET BANK VCC CA CLK DGND CA I&O CA DET
CN2003
9604S-12C
CN8503
9604S-12F
DGND CA DET NC CA CLK CA RESET CA VCC
CN8502
BKP1141
NC CA I&O NC DGND
CARD ASSY
(XWE1006)
C
SMART CARD
D+5V GND REM KEY_MENU KEY_OK KEY_LEFT KEY_UP KEY_DOWN KEY_RIGHT LED1 LED16 LED10 LED12 LED15 LED00 LED01 LED13 LED14 LED02 LED03
CN7002
9604S-21C
CN8401
PERSO S8402
VALIDER S8401
LEFT S8405
UP S8407
RIGHT S8406
S8404 DOWN

DBR-T210GBS, DBR-T210GBP
DBR-T210GBN

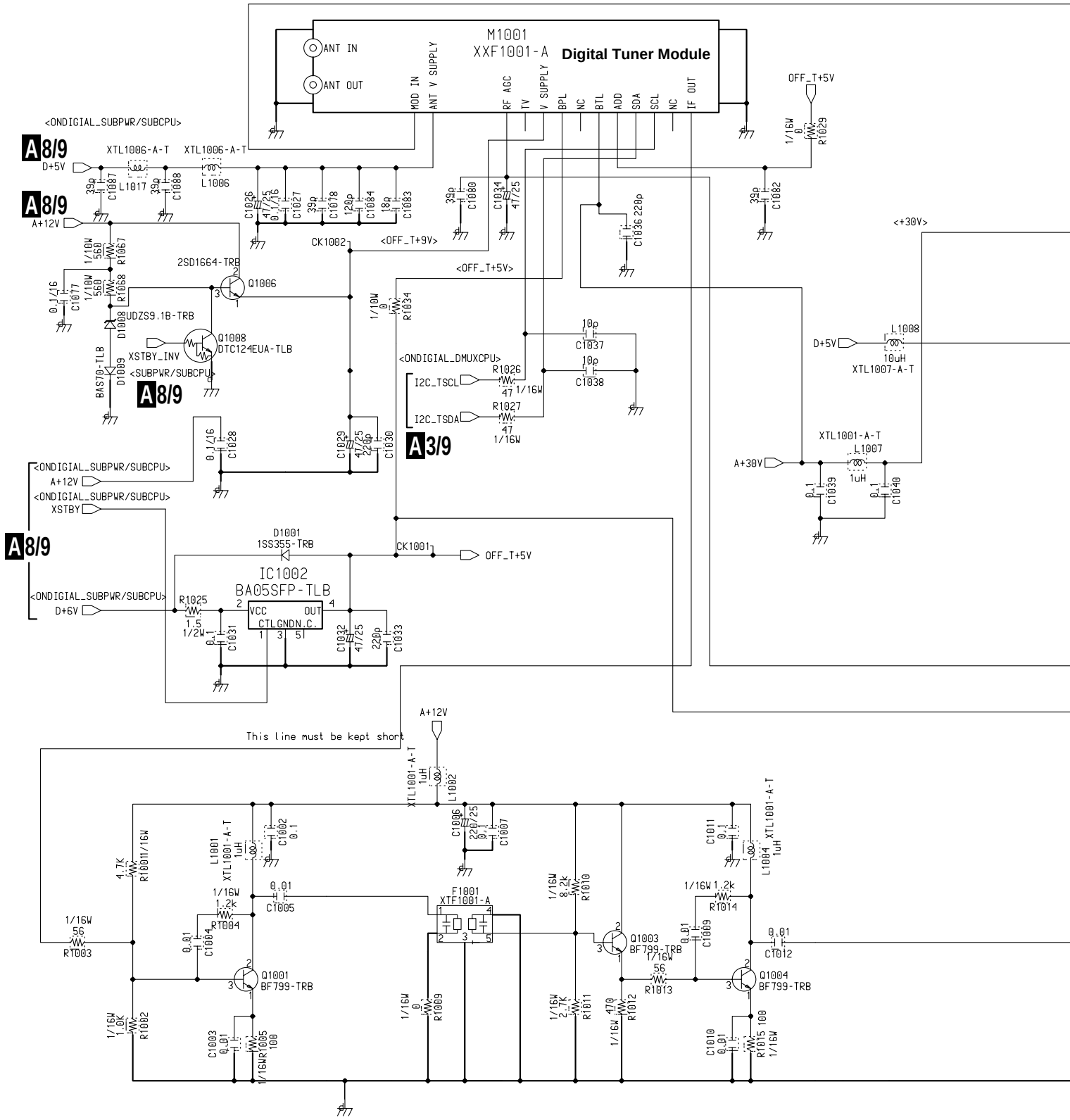
Note : When ordering service parts, be sure to refer to "EXPLODED VIEWS and PARTS LIST" or "PCB PARTS LIST".

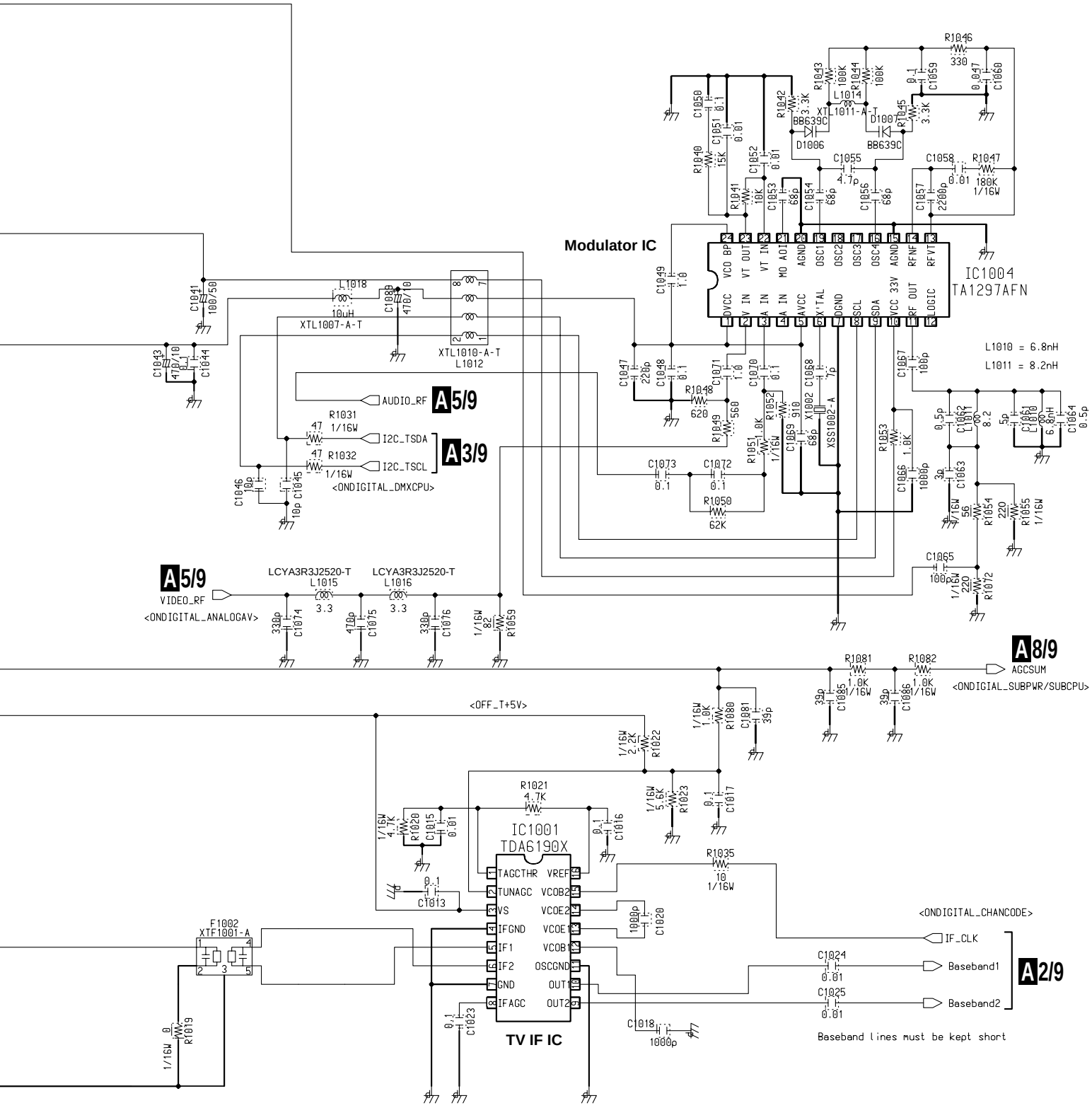




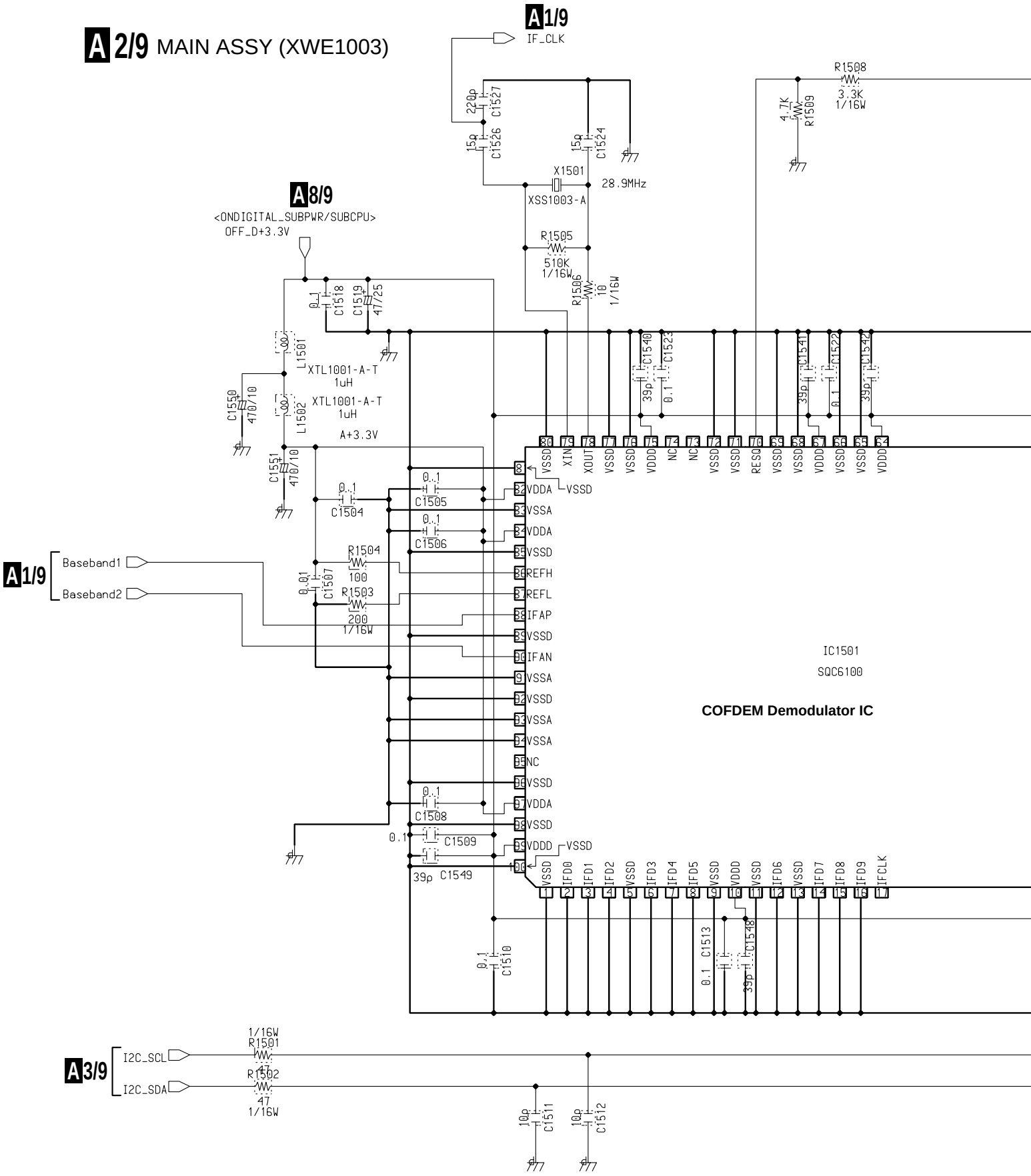
3.2 MAIN ASSY (1/9)

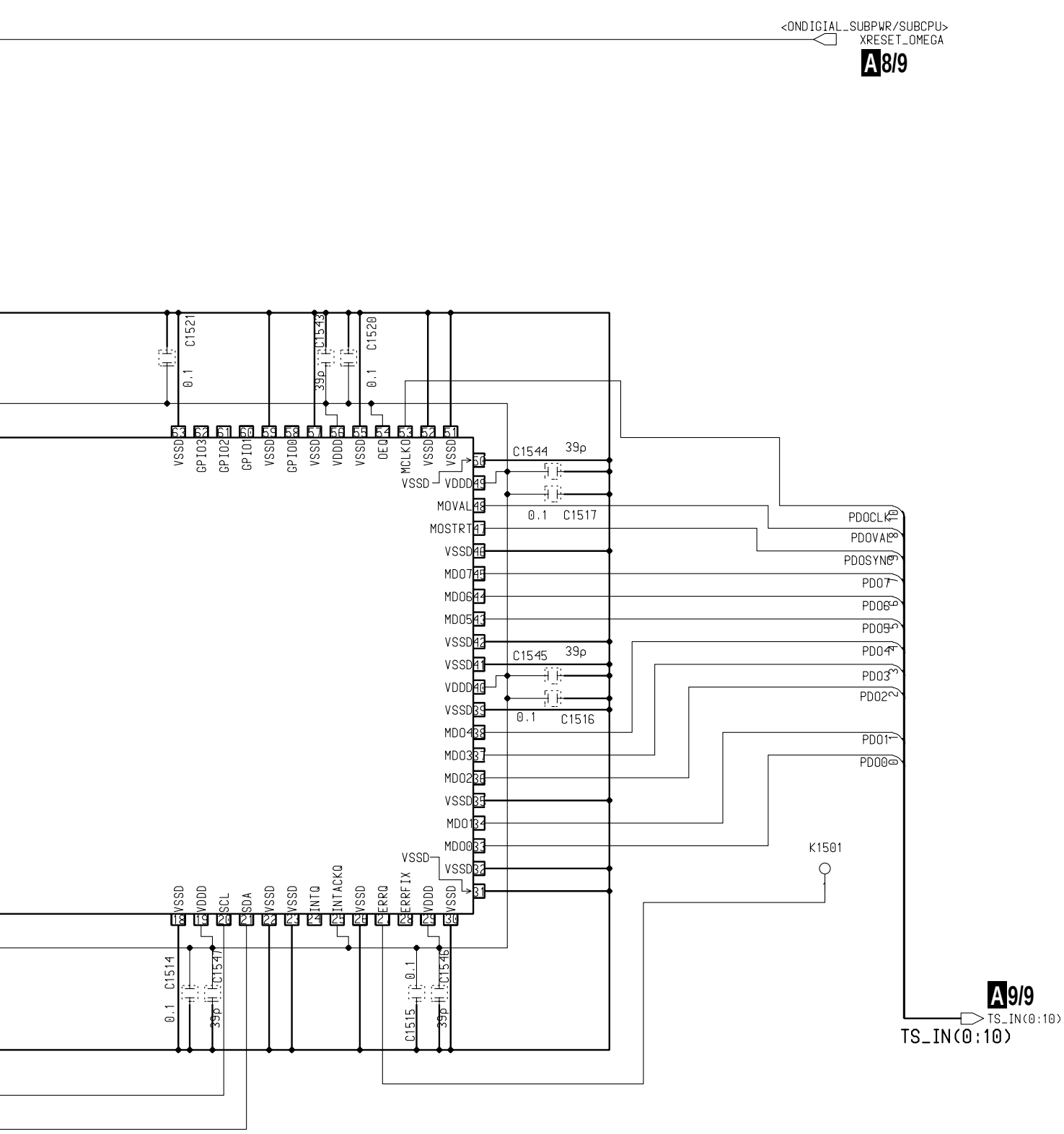
A 1/9 MAIN ASSY (XWE1003)



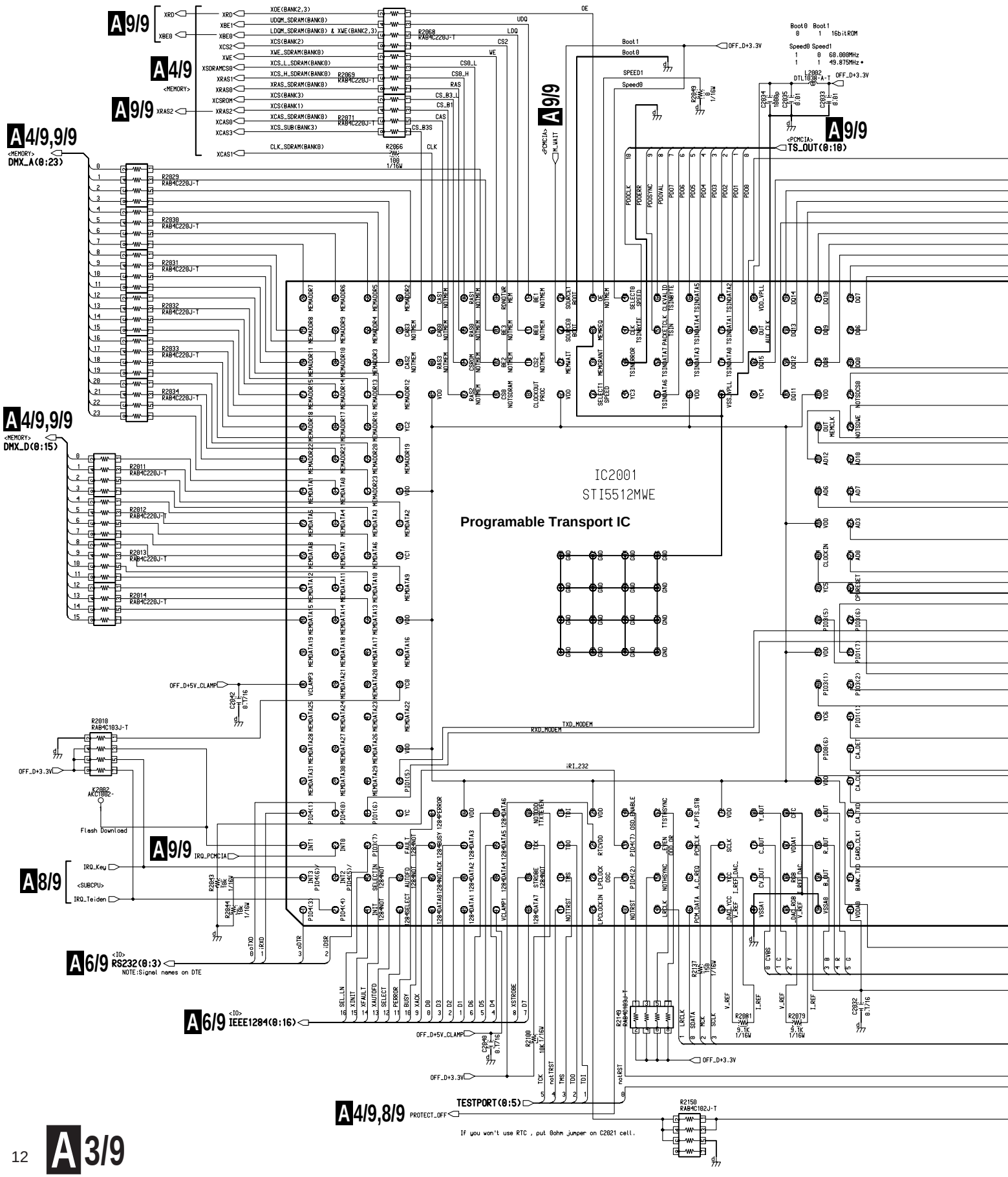

Modulator IC
IC1004
TA1297AFN
L1010 = 6.8nH
L1011 = 8.2nH
AUDIO_RF
A5/9
I2C_TSDA
I2C_TSCL
A3/9
<ONDIGITAL_DMXCPU>
VIDEO_RF
<ONDIGITAL_ANALOGAV>
LCYA3R3J2520-T
LCYA3R3J2520-T
A8/9
AGCSUM
<ONDIGITAL_SUBPWR/SUBCPU>
<OFF_T+5V>
IC1001
TDA6190X
TV IF IC
<ONDIGITAL_CHANCODE>
IF_CLK
Baseband1
Baseband2
A2/9
Baseband lines must be kept short

3.3 MAIN ASSY (2/9)

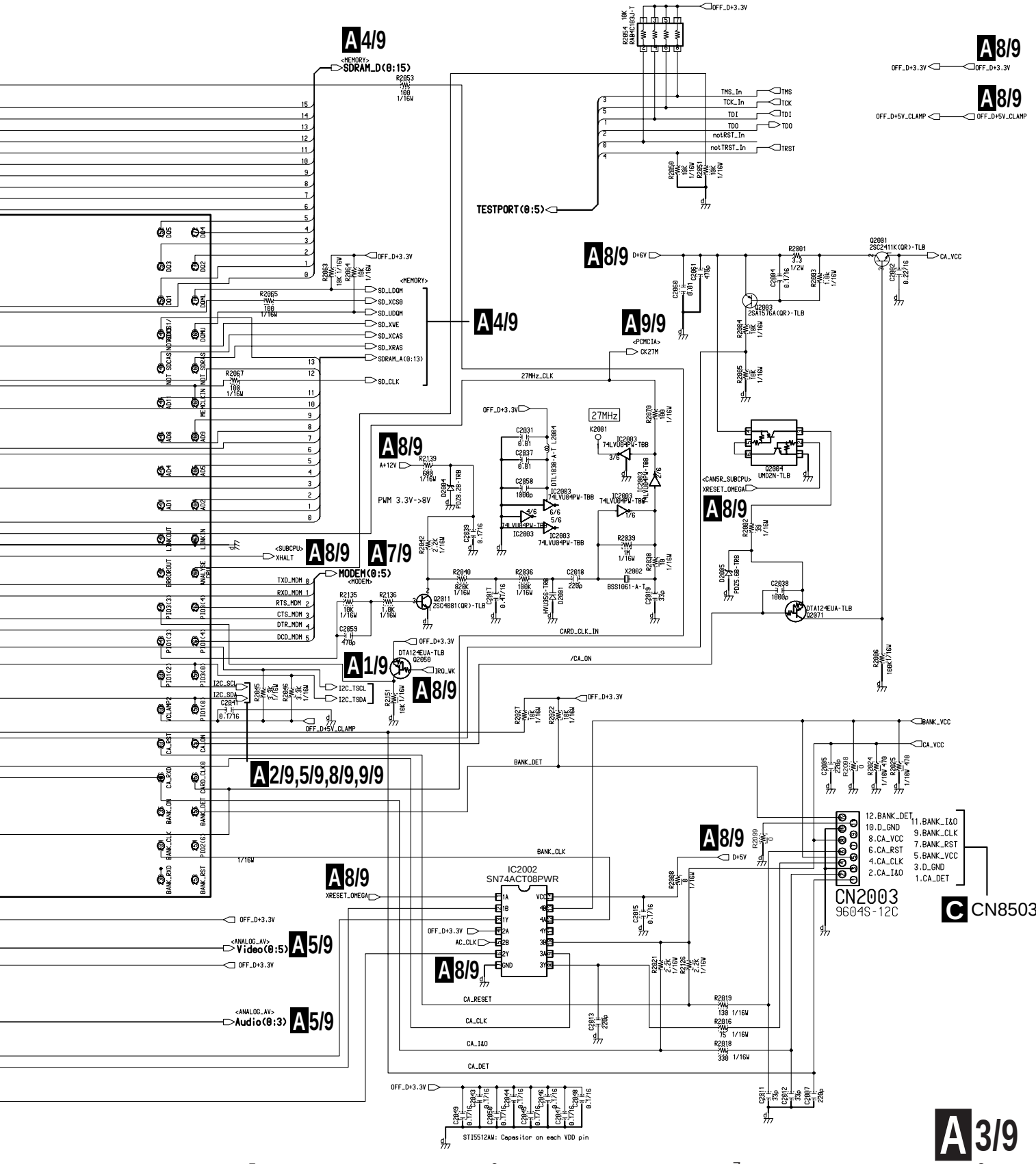



<ONDIGIAL_SUBPWR/SUBCPU>
XRESET_OMEGA
A8/9
C1521
C1543
C1520
C1544
C1517
C1545
C1516
C1514
C1547
C1515
C1546
K1501
PDOCLK
PDOVAL
PDOSYNC
PD07
PD06
PD05
PD04
PD03
PD02
PD01
PD00
A9/9
TS_IN(0:10)
TS_IN(0:10)

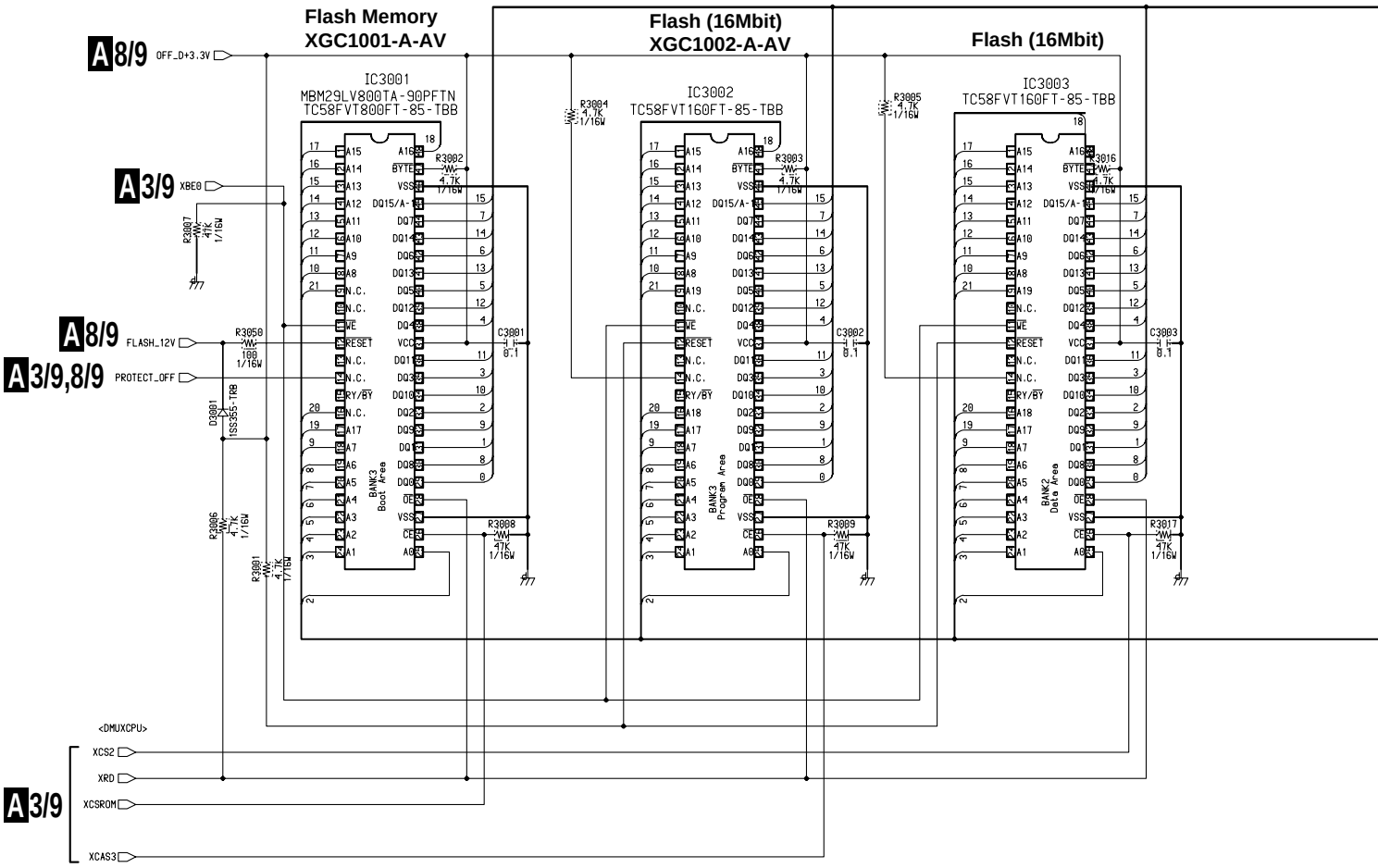
3.4 MAIN ASSY (3/9)



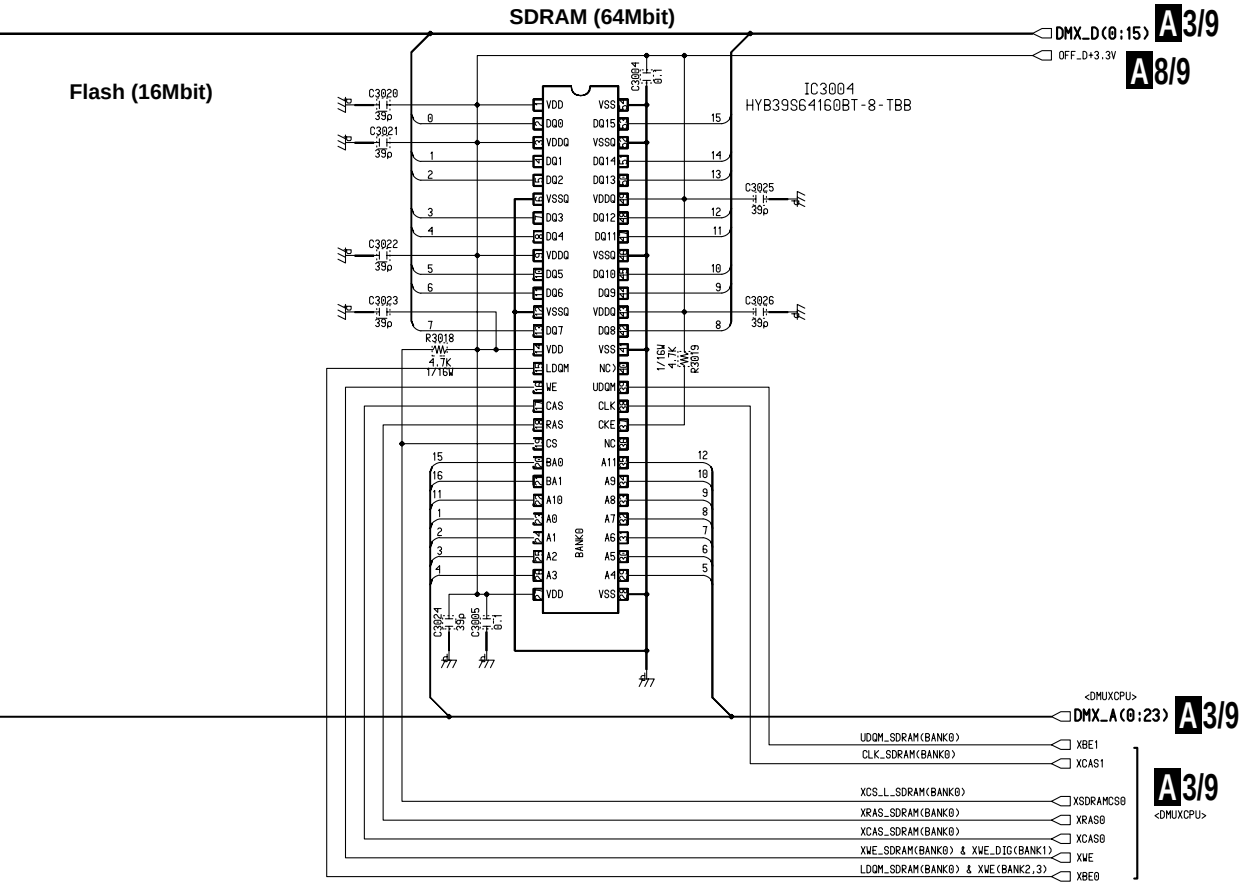
A 3/9 MAIN ASSY (XWE1003)

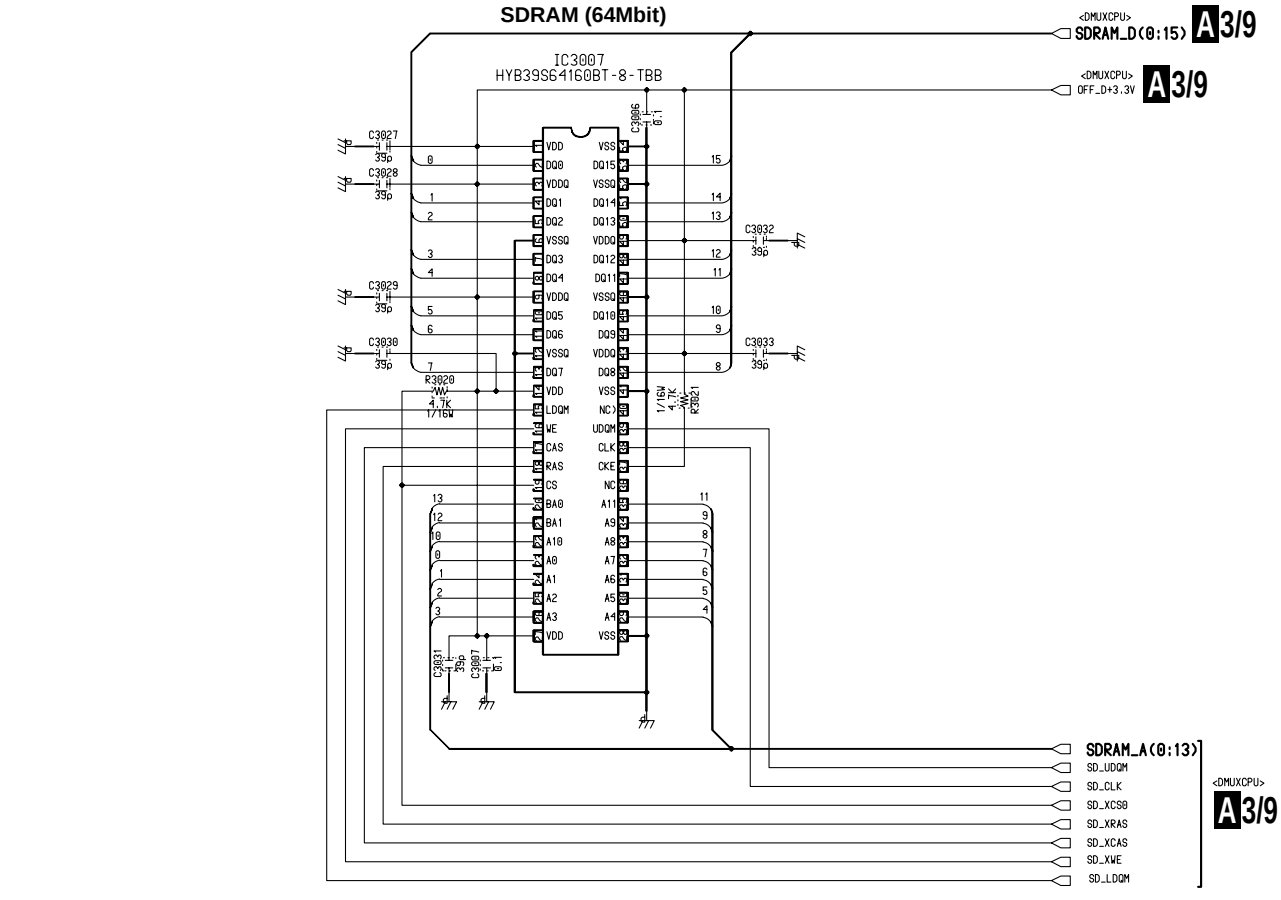


3.5 MAIN ASSY (4/9)

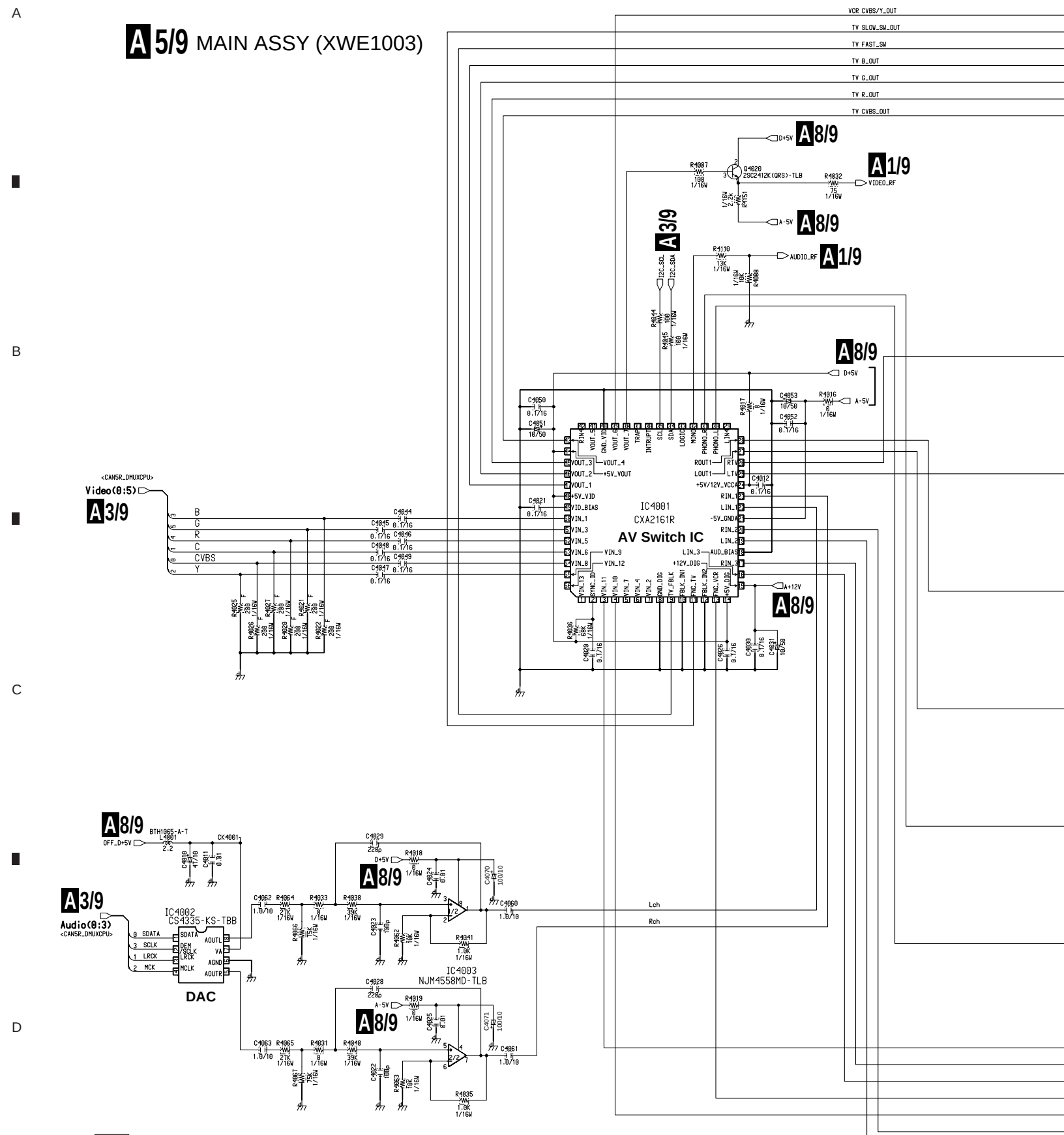


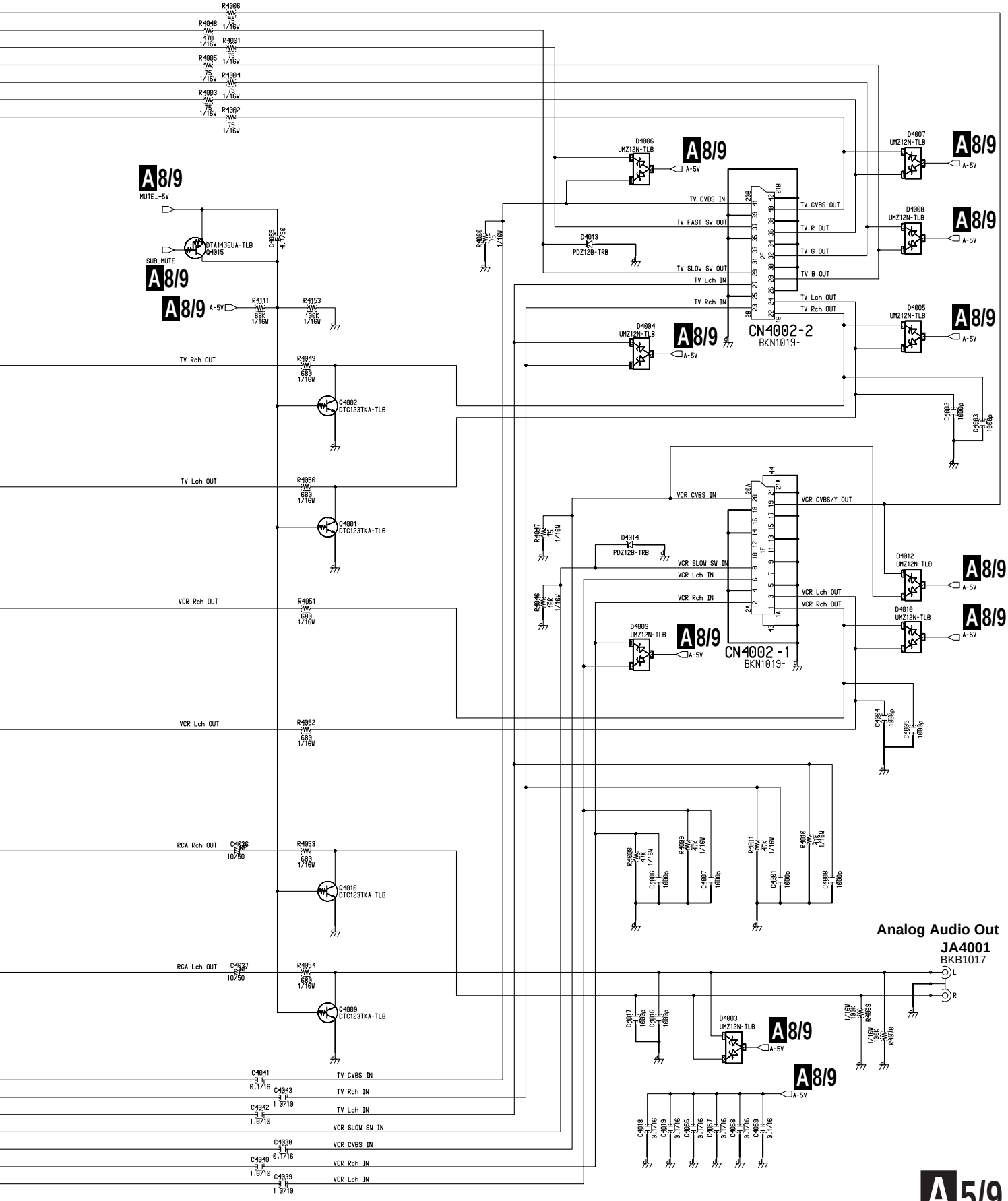
A 4/9 MAIN ASSY (XWE1003)


SDRAM (64Mbit)
Flash (16Mbit)
DMX_D(0:15) A3/9
OFF_D+3.3V A8/9
IC3004
HYB39S64160BT-8-TBB
C3020
C3021
C3022
C3023
C3025
C3026
C3004
R3018
4.7K
R3019
BANK0
C3024
C3005
<DMUXCPU>
DMX_A(0:23) A3/9
UDQM_SDRAM(BANK0)
CLK_SDRAM(BANK0)
XBE1
XCAS1
XCS_L_SDRAM(BANK0)
XRAS_SDRAM(BANK0)
XCAS_SDRAM(BANK0)
XWE_SDRAM(BANK0) & XWE_DIG(BANK1)
LDQM_SDRAM(BANK0) & XWE(BANK2,3)
XSDRAMCS0
XRAS0
XCAS0
XWE
XBE0
A3/9
<DMUXCPU>

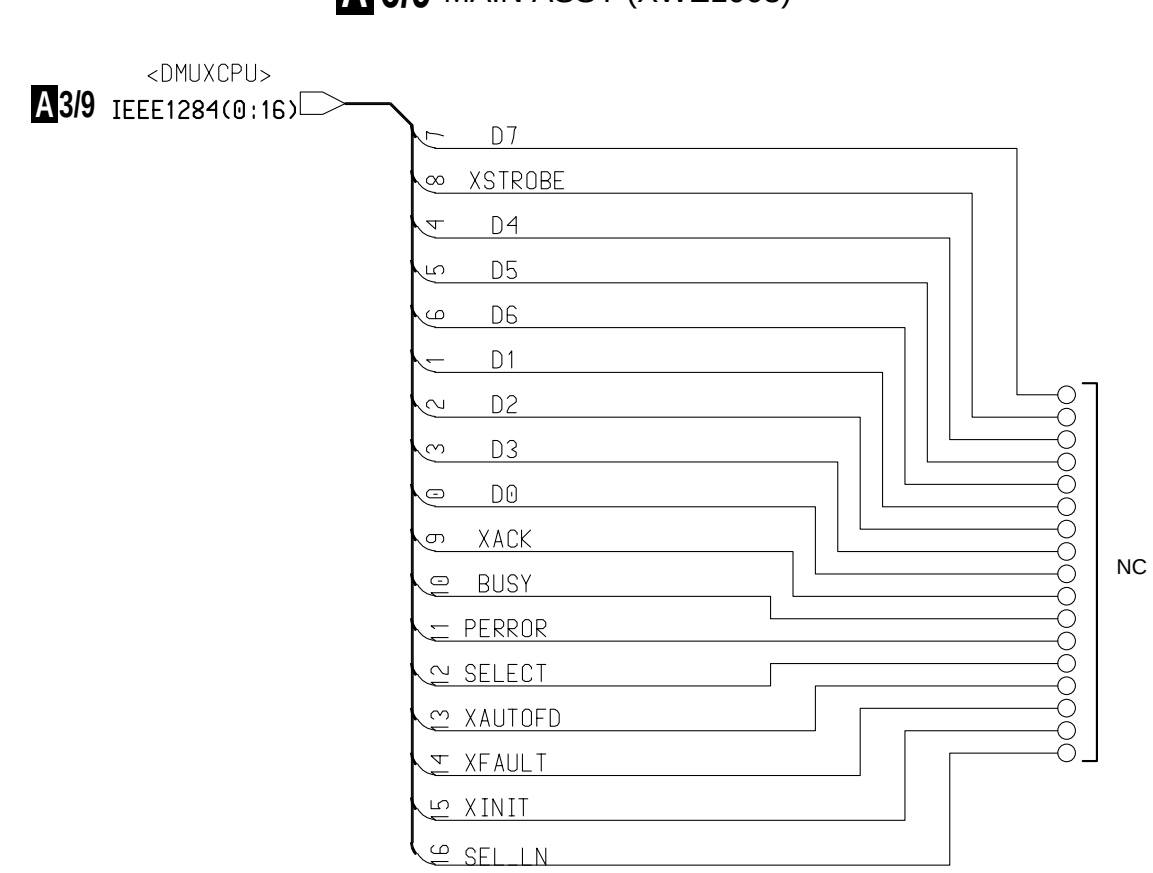

SDRAM (64Mbit)
IC3007
HYB39S64160BT-8-TBB
<DMUXCPU> SDRAM_D(0:15) A3/9
<DMUXCPU> OFF_D+3.3V A3/9
C3027
C3028
C3029
C3030
C3032
C3033
C3006
R3020
4.7K
R3021
BANK0
C3031
C3007
SDRAM_A(0:13)
SD_UDQM
SD_CLK
SD_XCS0
SD_XRAS
SD_XCAS
SD_XWE
SD_LDQM
<DMUXCPU>
A3/9

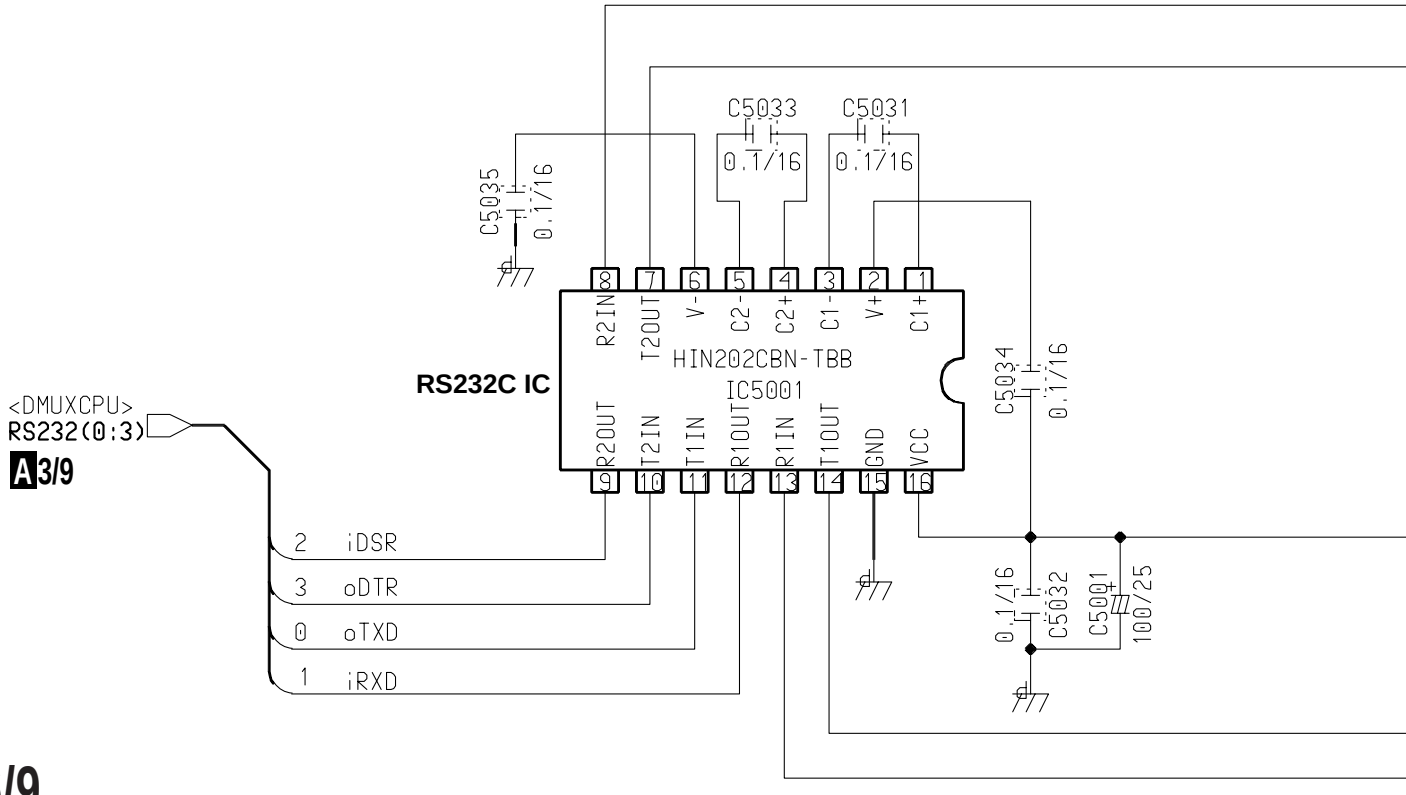
3.6 MAIN ASSY (5/9)

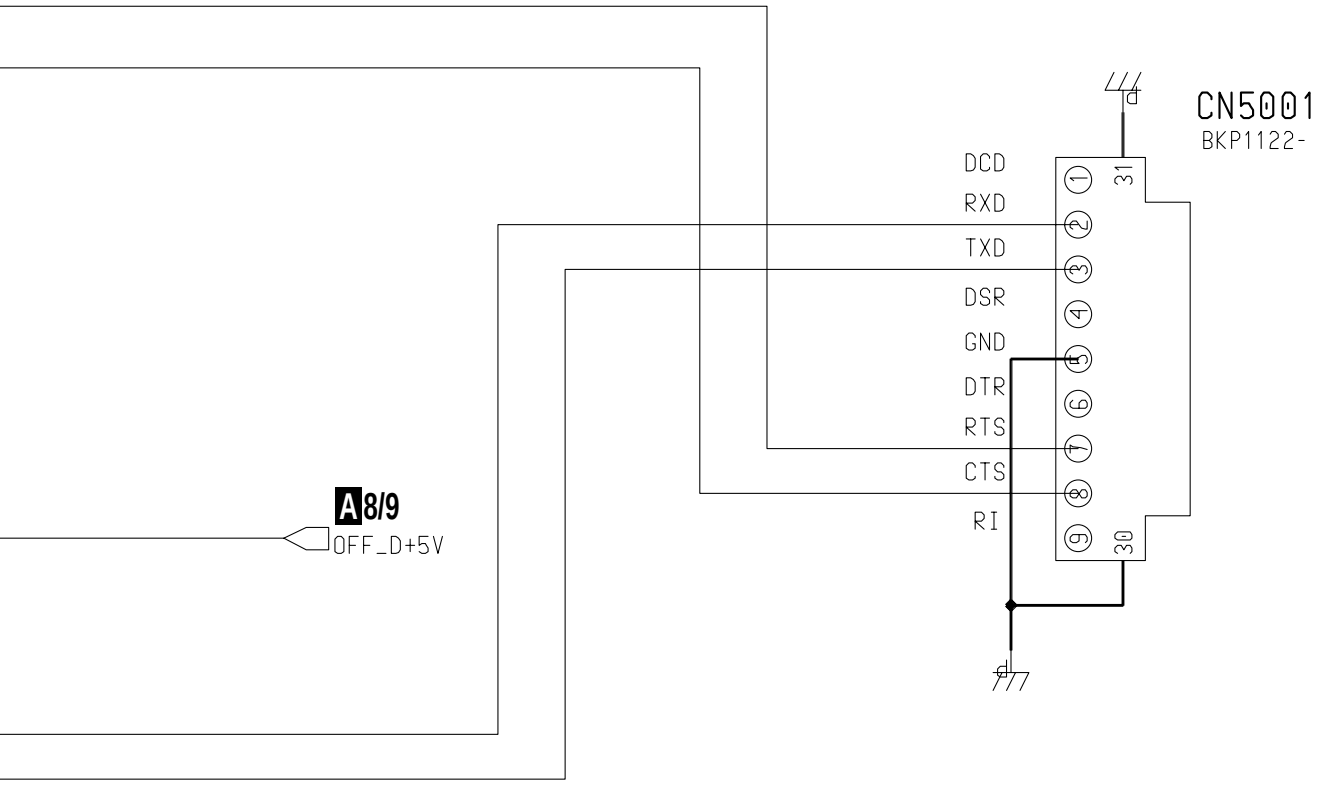



CN4002-2
BKN1019-
CN4002-1
BKN1019-
TV CVBS IN
TV FAST SW OUT
TV SLOW SW OUT
TV Lch IN
TV Rch IN
TV CVBS OUT
TV R OUT
TV G OUT
TV B OUT
TV Lch OUT
TV Rch OUT
VCR CVBS IN
VCR SLOW SW IN
VCR Lch IN
VCR Rch IN
VCR CVBS/Y OUT
VCR Lch OUT
VCR Rch OUT
MUTE_+5V
SUB_MUTE
A-5V
TV Rch OUT
TV Lch OUT
VCR Rch OUT
VCR Lch OUT
RCA Rch OUT
RCA Lch OUT
Analog Audio Out
JA4001
BKB1017
L
R

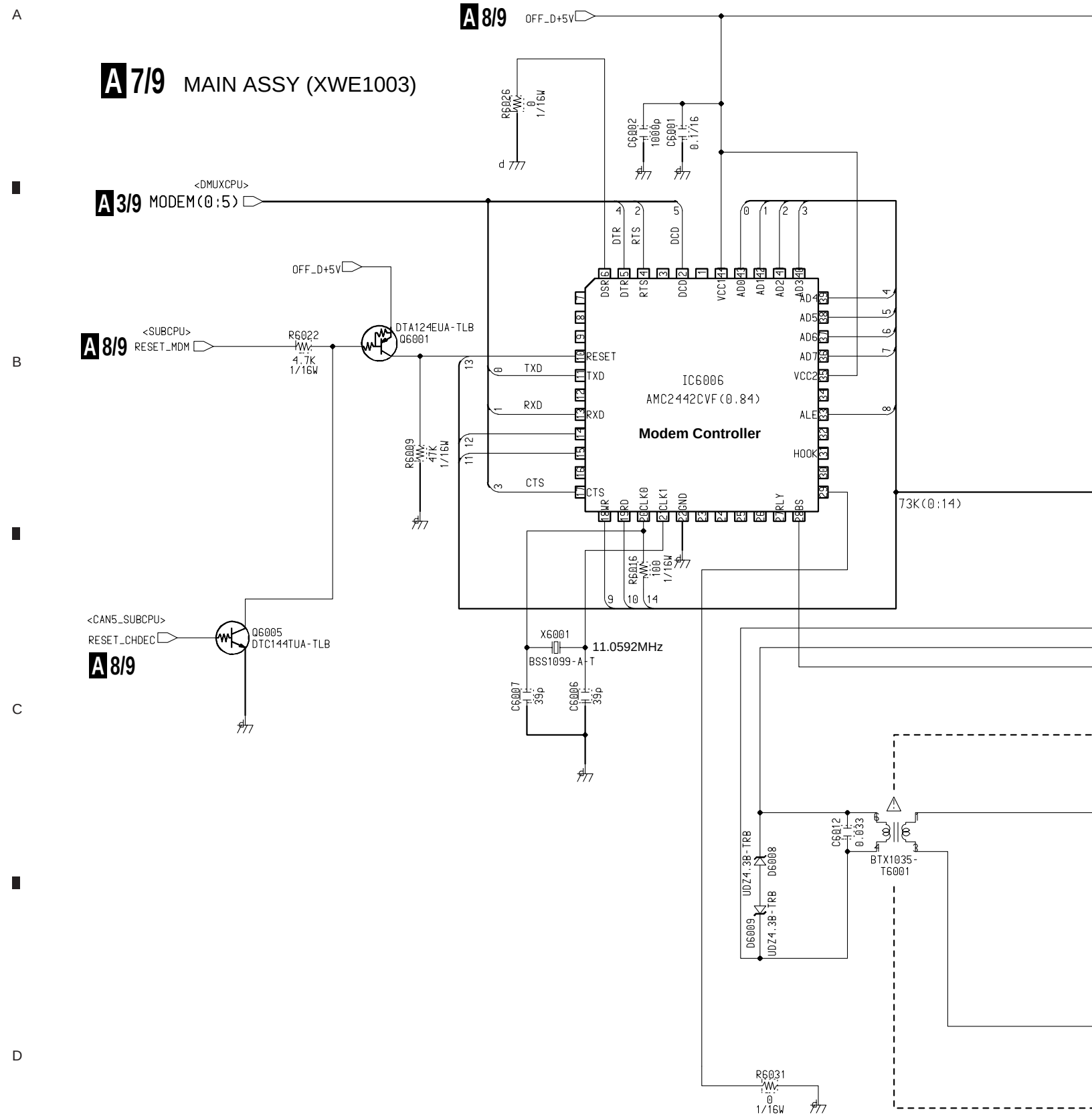
3.7 MAIN ASSY (6/9)

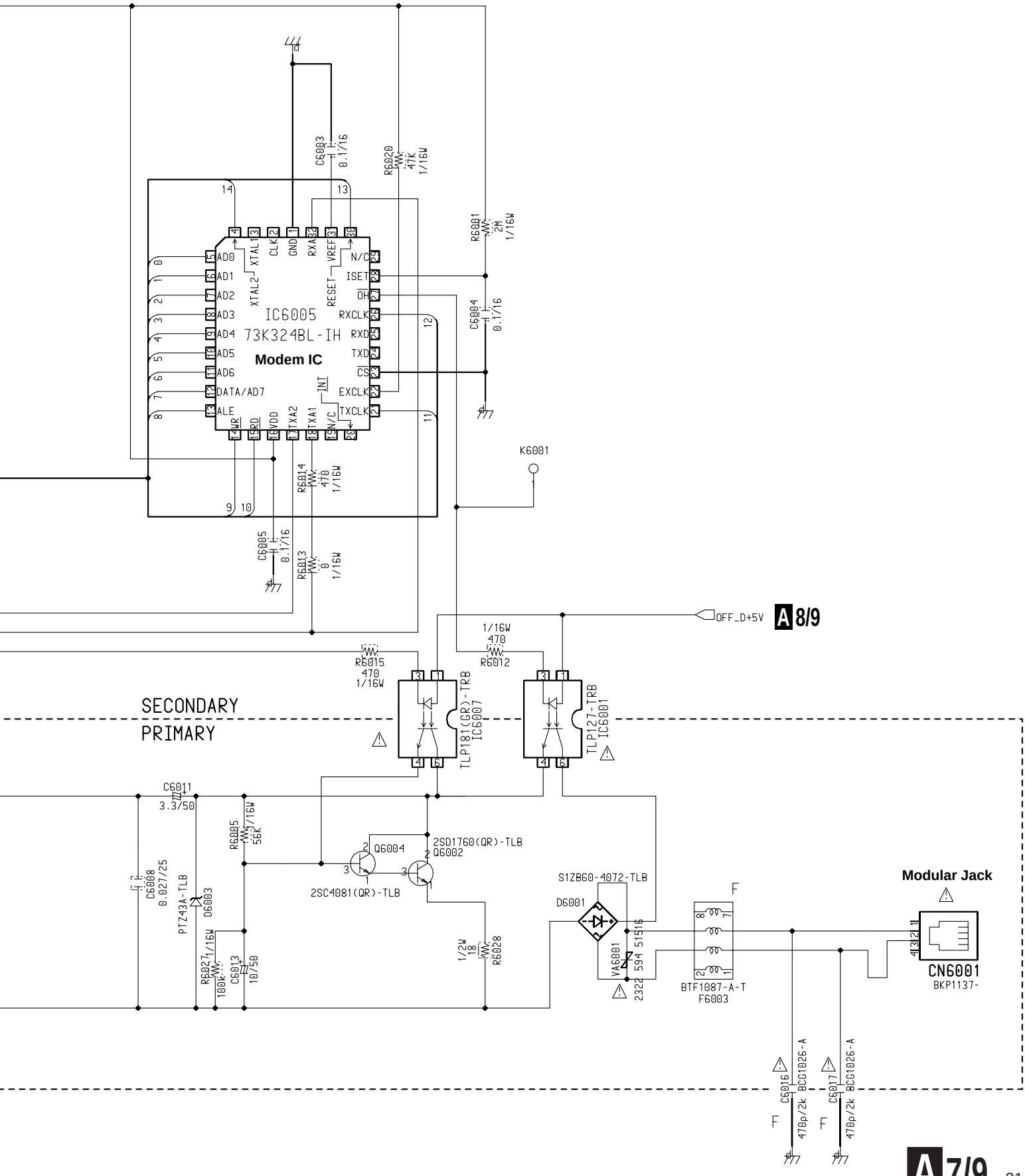




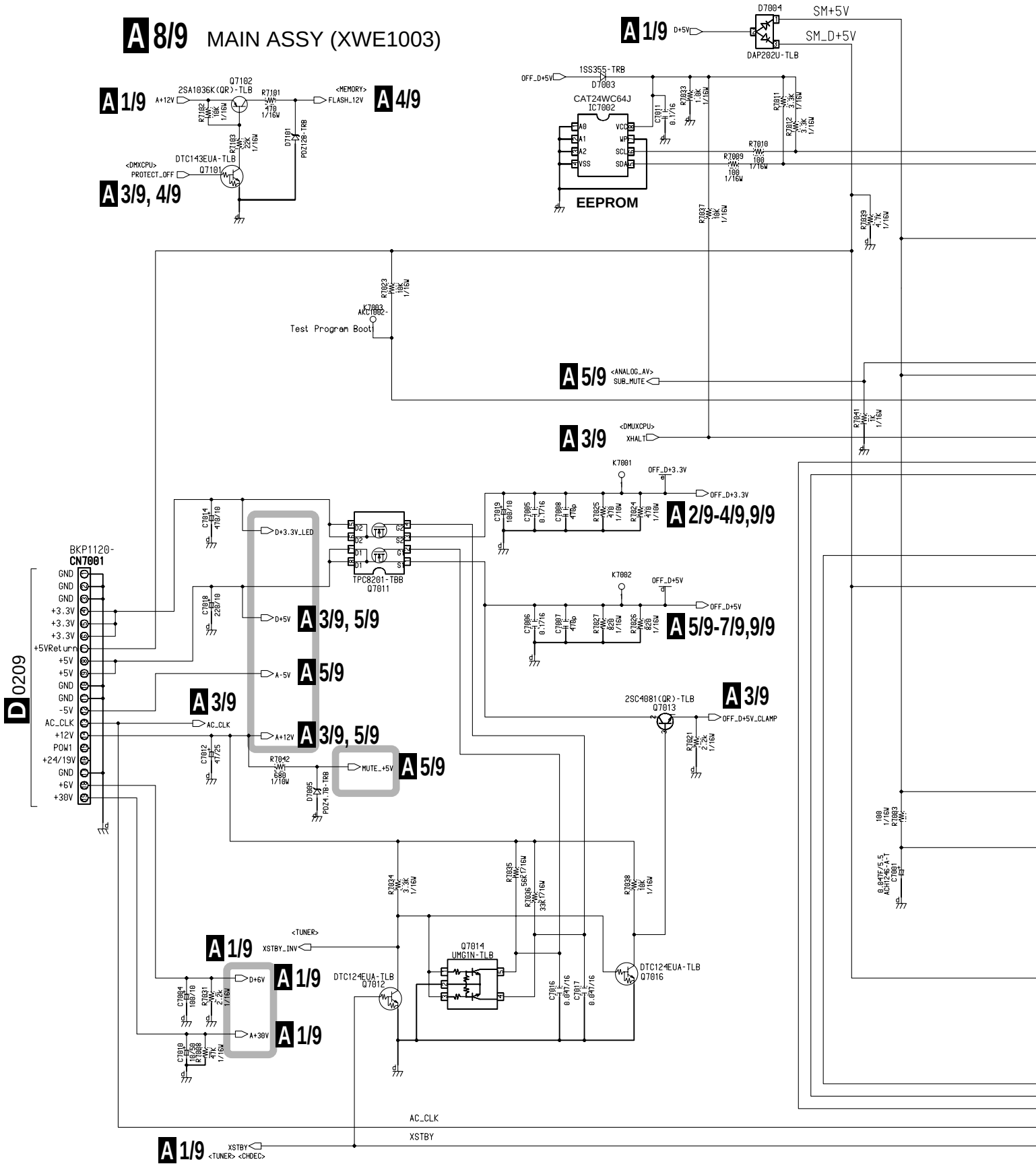

CN5001
BKP1122-
DCD
RXD
TXD
DSR
GND
DTR
RTS
CTS
RI
31
30
1
2
3
4
5
6
7
8
9
A8/9
OFF_D+5V

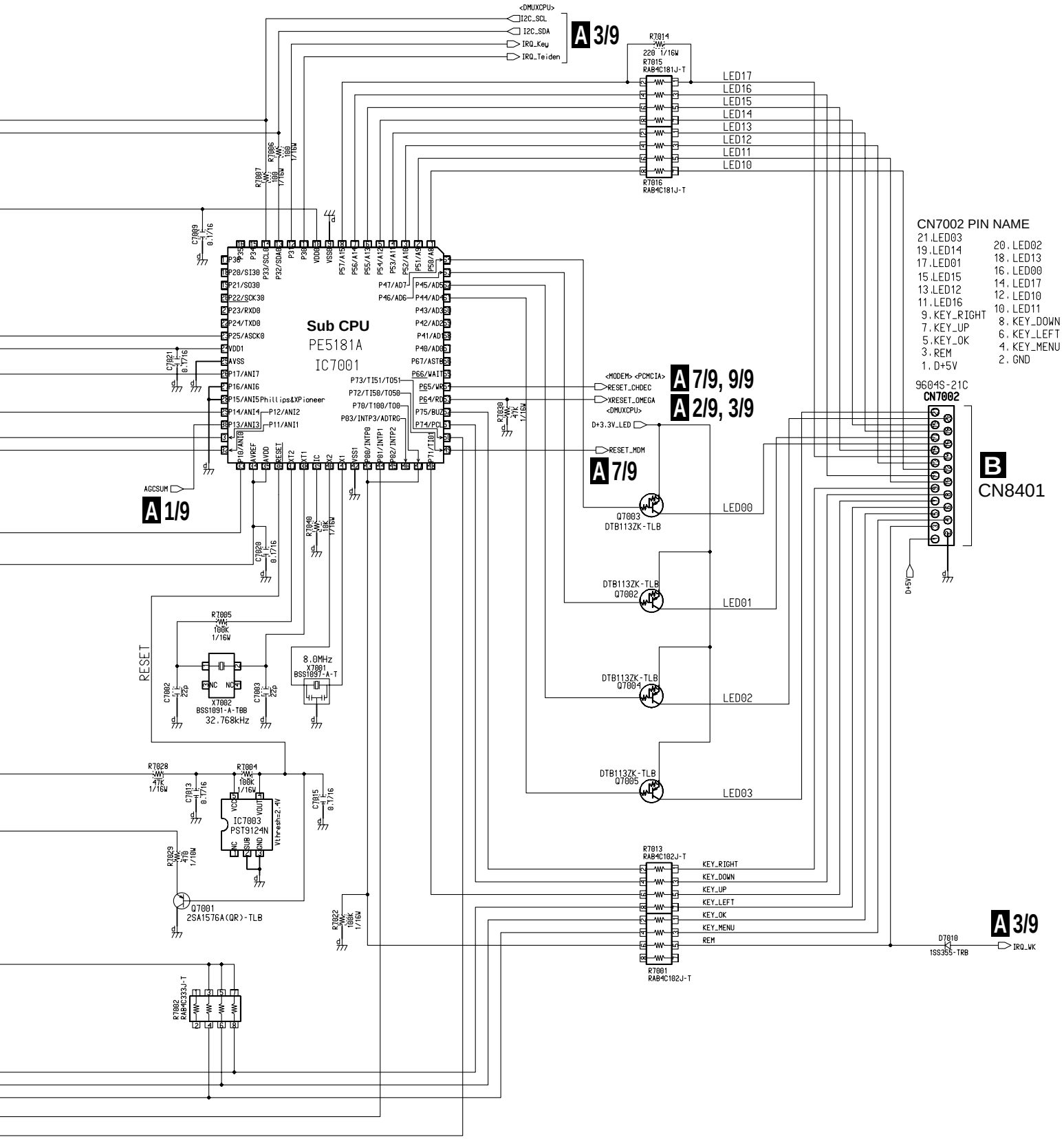
3.8 MAIN ASSY (7/9)



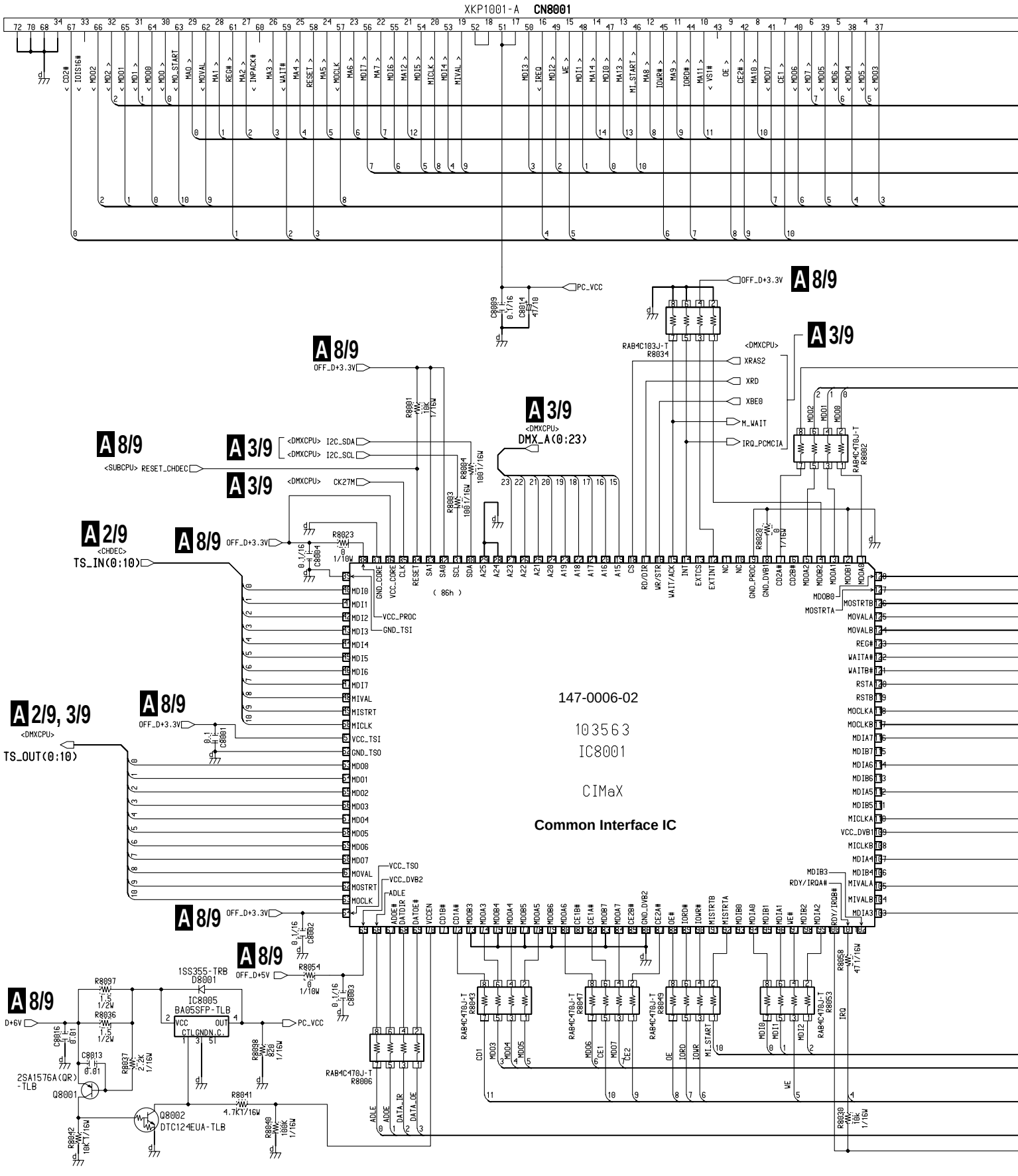

IC6005
73K324BL-IH
Modem IC
AD0
AD1
AD2
AD3
AD4
AD5
AD6
DATA/AD7
ALE
XTAL1
XTAL2
CLK
GND
RXA
VREF
N/C
ISET
RESET
OH
RXCLK
RXD
TXD
CS
INT
EXCLK
TXCLK
WR
RD
VDD
TXA2
TXA1
N/C
C6003 0.1/16
R6020 47K 1/16W
R6001 2M 1/16W
C6004 0.1/16
K6001
R6014 470 1/16W
C6005 0.1/16
R6013 0 1/16W
OFF_D+5V
A 8/9
R6015 470 1/16W
R6012 1/16W 470
TLP181(GR)-TRB IC6007
TLP127-TRB IC6001
SECONDARY
PRIMARY
C6011 3.3/50
R6005 1/16W 56K
Q6004
2SD1760(QR)-TLB Q6002
2SC4081(QR)-TLB
C6008 0.027/25
PTZ43A-TLB
D6003
R6027 1/16W 100K
C6013 10/50
1/2W 18
R6028
S1ZB60-4072-TLB
D6001
VA6001
BTF1087-A-T F6003
Modular Jack
CN6001 BKP1137-
C6016 470p/2k BCG1026-A
C6017 470p/2k BCG1026-A

3.9 MAIN ASSY (8/9)

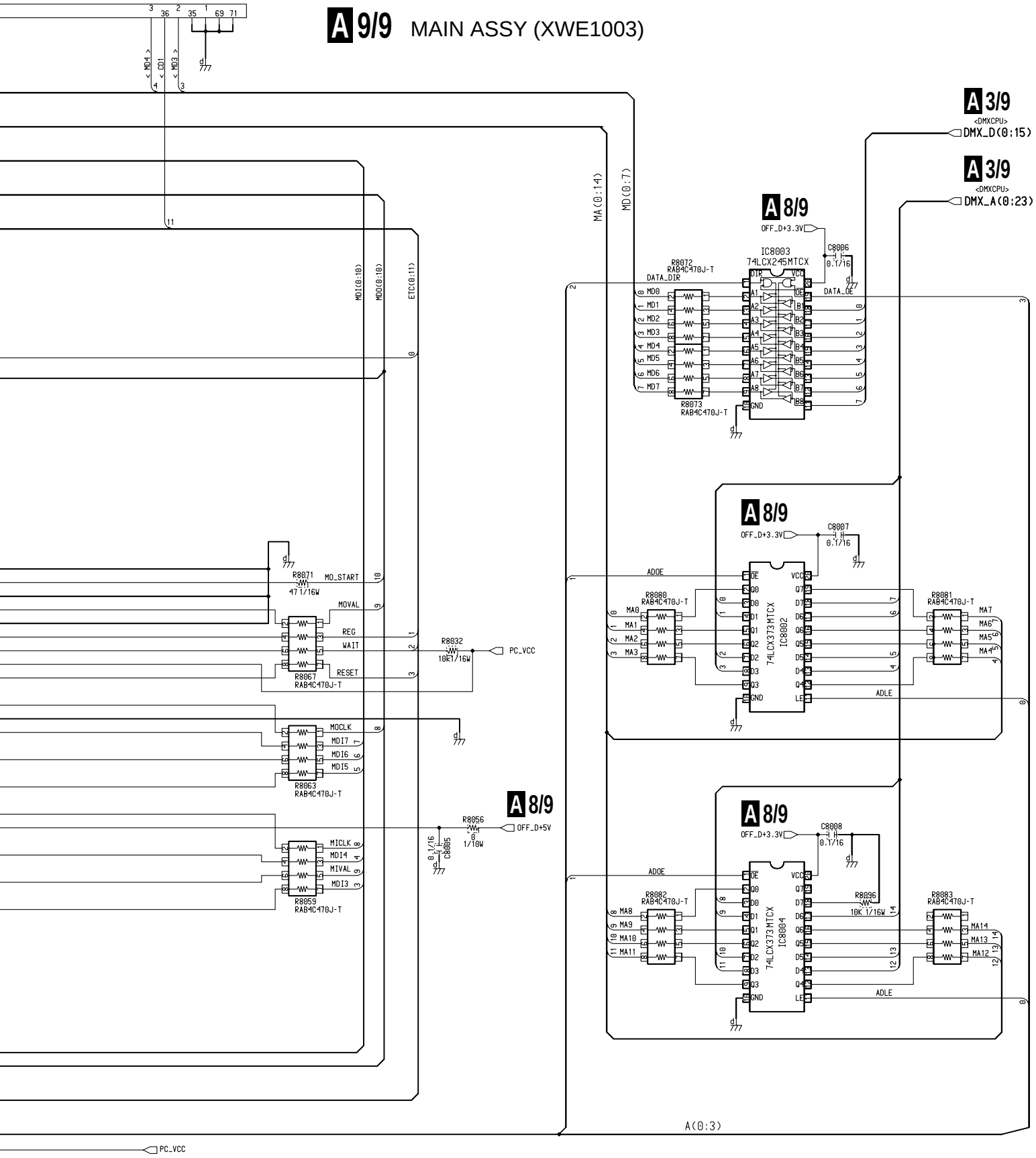



<DMUXCPU>
I2C_SCL
I2C_SDA
IRQ_Key
IRQ_Teiden
A 3/9
R7014
220 1/16W
R7015
RAB4C181J-T
LED17
LED16
LED15
LED14
LED13
LED12
LED11
LED10
R7016
RAB4C181J-T
R7006
100
1/16W
R7007
100
1/16W
C7009
0.1/16
Sub CPU
PE5181A
IC7001
P30
P20/SI30
P21/SO30
P22/SCK30
P23/RXD0
P24/TXD0
P25/ASCK0
VDD1
AVSS
P17/ANI7
P16/ANI6
P15/ANI5
P14/ANI4
P13/ANI3
P12/ANI2
P11/ANI1
P10/ANI0
AVREF
AVDD
RESET
XT2
XT1
IC
X2
X1
VSS1
P00/INTP0
P01/INTP1
P02/INTP2
P71/TI01
P70/TI00/TO0
P03/INTP3/ADTRG
P72/TI50/TO50
P73/TI51/TO51
P47/AD7
P46/AD6
P45/AD5
P44/AD4
P43/AD3
P42/AD2
P41/AD1
P40/AD0
P67/ASTB
P66/WAIT
P65/WR
P64/RD
P75/BUZ
P74/PCL
P51/A9
P50/A8
P57/A15
P56/A14
P55/A13
P54/A12
P53/A11
P52/A10
P33/SCL0
P32/SDA0
P31
P30
VDD0
VSS0
C7021
0.1/16
C7020
0.1/16
R7040
10K
1/16W
R7030
47K
1/16W
AGCSUM
A 1/9
<MODEM> <PCMCIA>
RESET_CHDEC
XRESET_OMEGA
<DMUXCPU>
D+3.3V_LED
RESET_MDM
A 7/9, 9/9
A 2/9, 3/9
A 7/9
Q7003
DTB113ZK-TLB
LED00
DTB113ZK-TLB
Q7002
LED01
DTB113ZK-TLB
Q7004
LED02
DTB113ZK-TLB
Q7005
LED03
CN7002 PIN NAME
21.LED03
19.LED14
17.LED01
15.LED15
13.LED12
11.LED16
9.KEY_RIGHT
7.KEY_UP
5.KEY_OK
3.REM
1.D+5V
20.LED02
18.LED13
16.LED00
14.LED17
12.LED10
10.LED11
8.KEY_DOWN
6.KEY_LEFT
4.KEY_MENU
2.GND
9604S-21C
CN7002
B
CN8401
D+5V
R7005
100K
1/16W
RESET
8.0MHz
X7001
BSS1097-A-T
C7002
22p
C7003
22p
X7002
BSS1091-A-TBB
32.768kHz
R7028
47K
1/16W
R7004
100K
1/16W
C7013
0.1/16
C7015
0.1/16
IC7003
PST9124N
Vthresh=2.4V
R7029
47K
1/16W
Q7001
2SA1576A(QR)-TLB
R7022
100K
1/16W
R7013
RAB4C102J-T
KEY_RIGHT
KEY_DOWN
KEY_UP
KEY_LEFT
KEY_OK
KEY_MENU
REM
R7001
RAB4C102J-T
D7010
1SS355-TRB
A 3/9
IRQ_WK
R7002
RAB4C333J-T

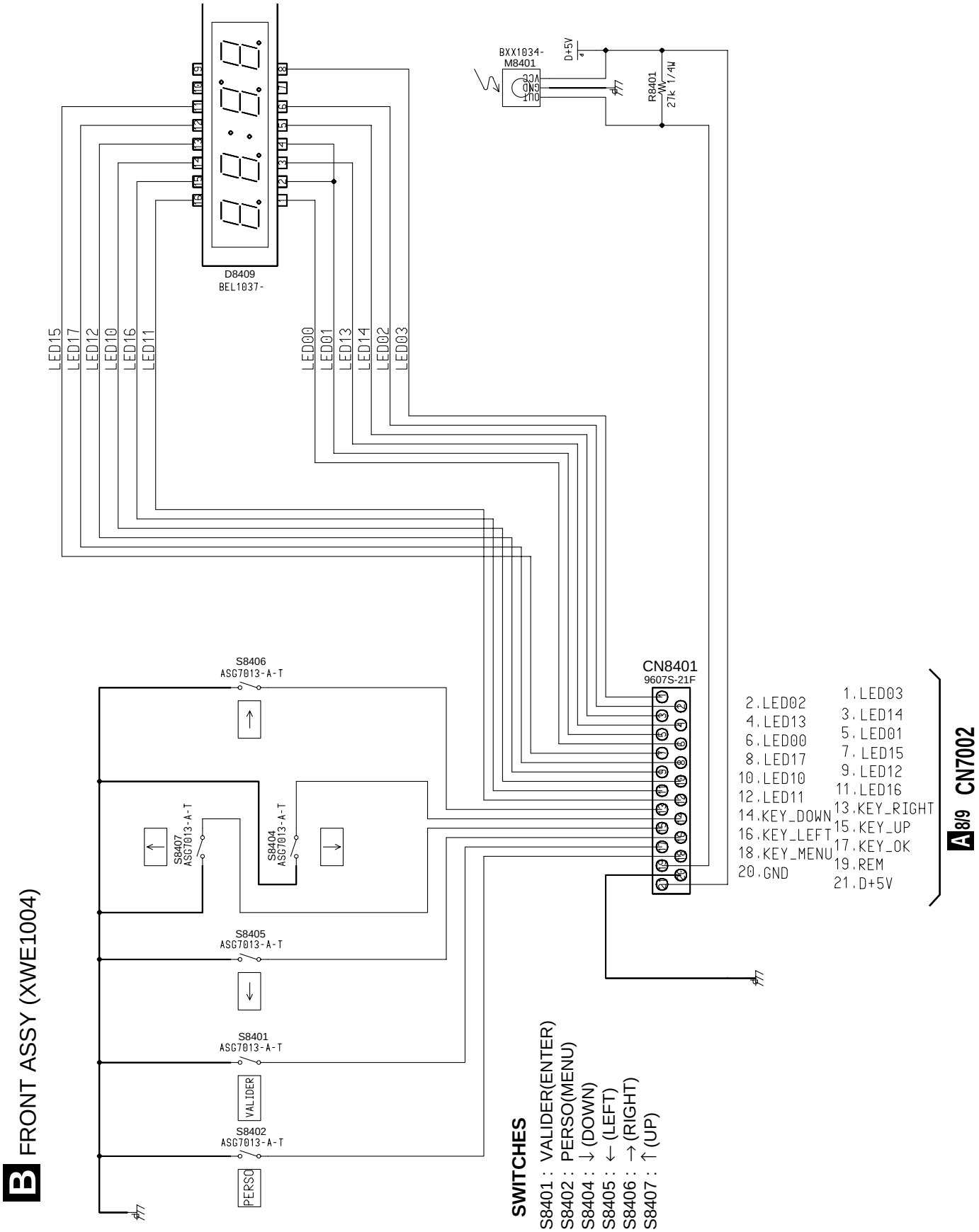
3.10 MAIN ASSY (9/9)



A 9/9 MAIN ASSY (XWE1003)



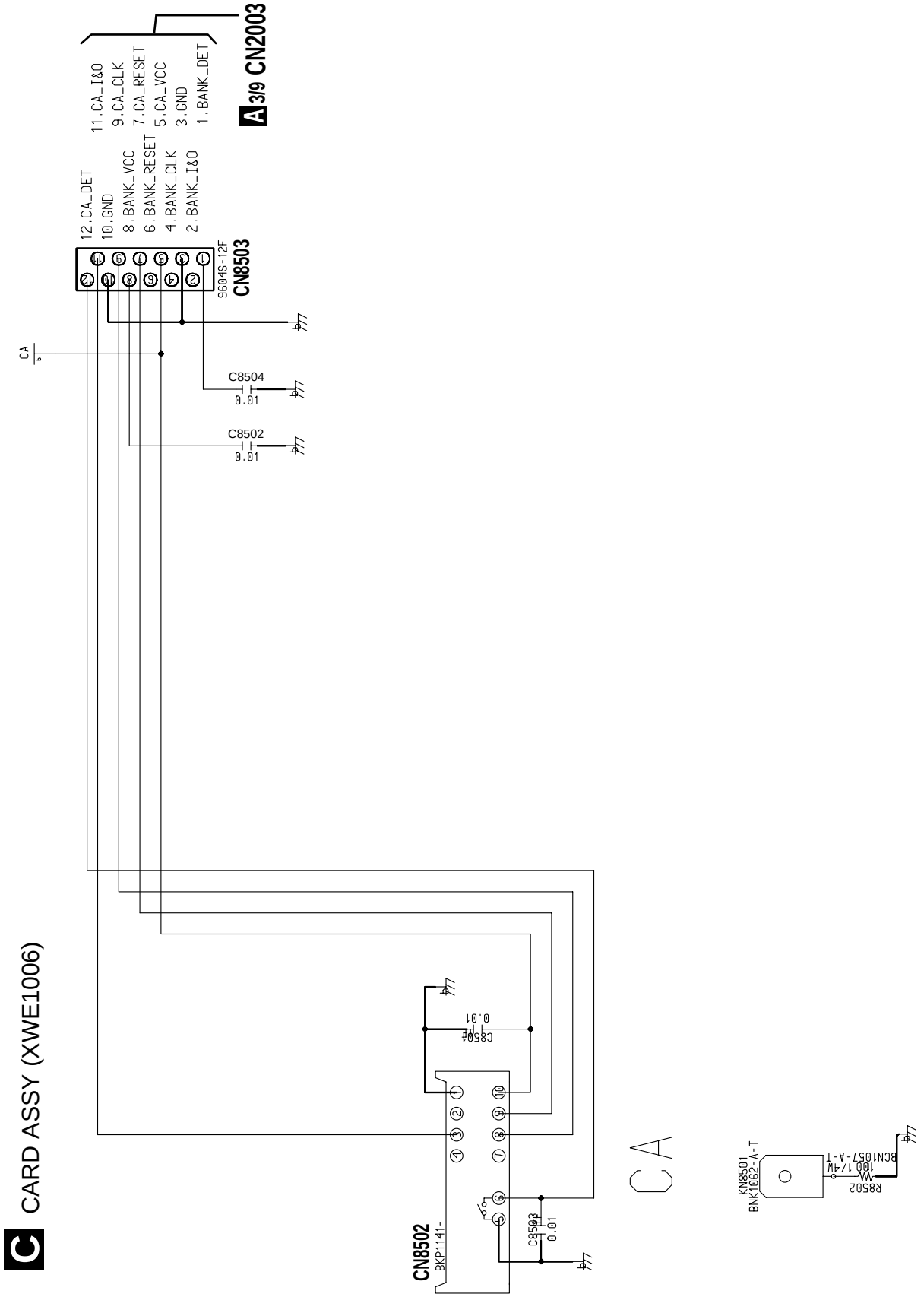
3.11 FRONT ASSY



SWITCHES

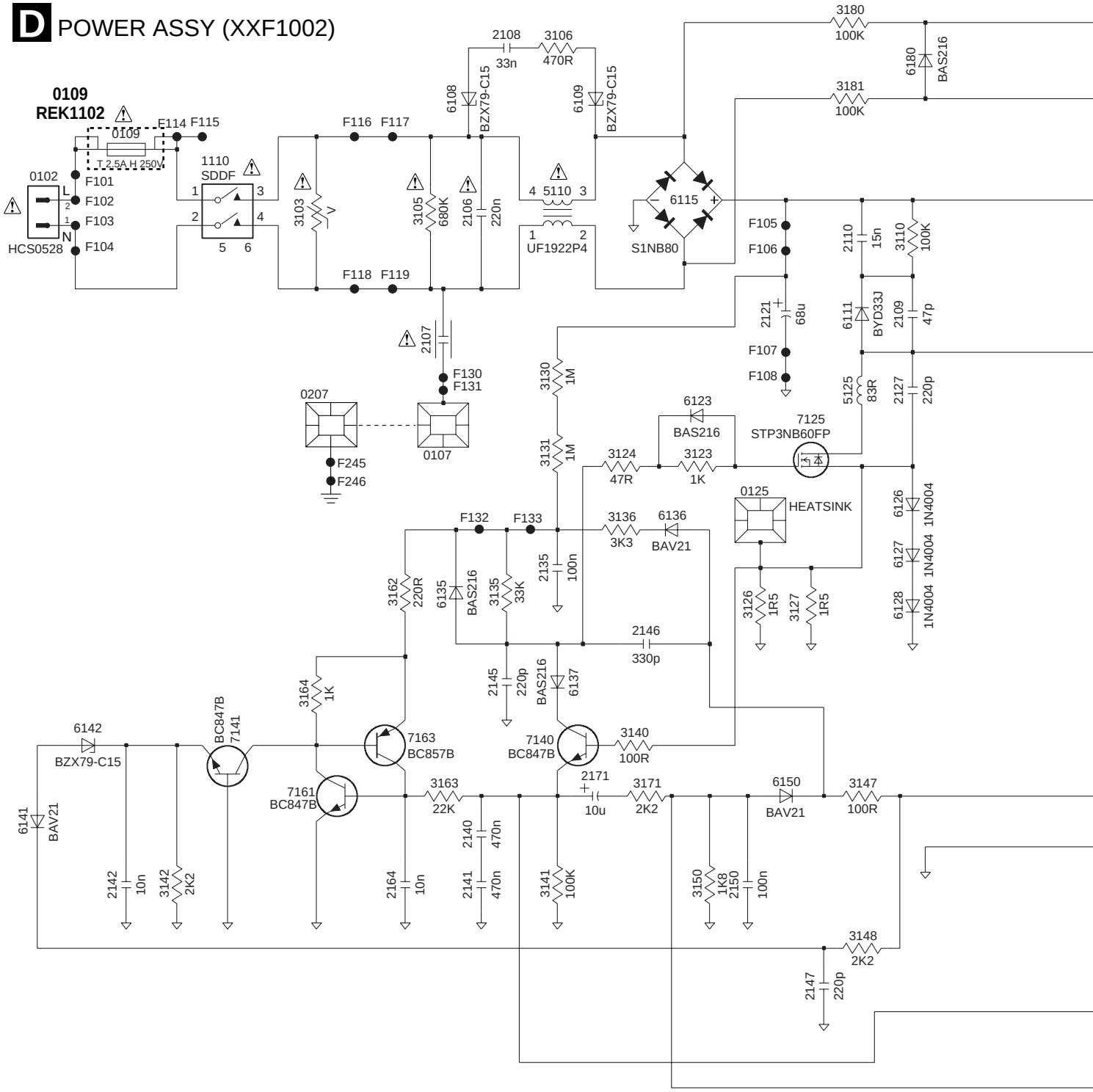
S8401 : VALIDER(ENTER)
S8402 : PERSO(MENU)
S8404 : ↓ (DOWN)
S8405 : ← (LEFT)
S8406 : → (RIGHT)
S8407 : ↑ (UP)

3.12 CARD ASSY



3.13 POWER ASSY

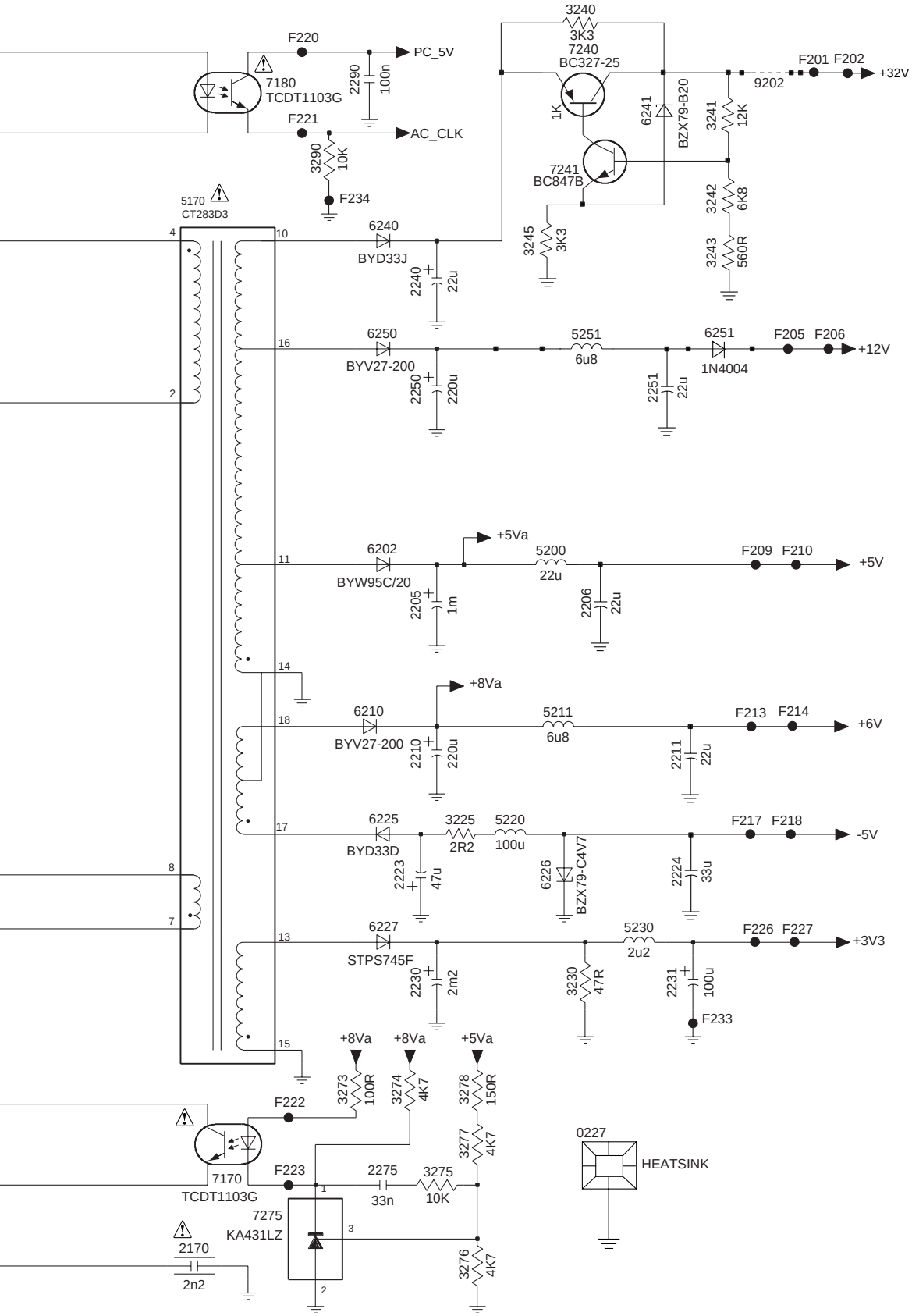
D POWER ASSY (XXF1002)

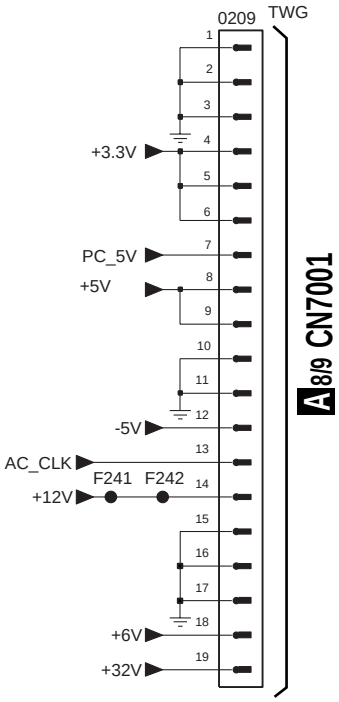


Fuse 0109 (REK1102) : Only this part is supplied as a service part..

● NOTE FOR FUSE REPLACEMENT

CAUTION – FOR CONTINUED PROTECTION AGAINST RISK OF FIRE.
REPLACE ONLY WITH SAME TYPE AND RATINGS ONLY.


F220
PC_5V
7180
TCDT1103G
2290
100n
F221
AC_CLK
3290
10K
F234
5170
CT283D3
3240
3K3
7240
BC327-25
1K
6241
BZX79-B20
3241
12K
F201 F202
+32V
9202
7241
BC847B
3242
6K8
3243
560R
3245
3K3
6240
BYD33J
2240
22u
6250
BYV27-200
2250
220u
5251
6u8
6251
1N4004
2251
22u
F205 F206
+12V
6202
BYW95C/20
2205
1m
+5Va
5200
22u
2206
22u
F209 F210
+5V
6210
BYV27-200
2210
220u
+8Va
5211
6u8
2211
22u
F213 F214
+6V
6225
BYD33D
3225
2R2
5220
100u
2223
47u
6226
BZX79-C4V7
2224
33u
F217 F218
-5V
6227
STPS745F
2230
2m2
5230
2u2
3230
47R
2231
100u
F233
F226 F227
+3V3
+8Va
+8Va
+5Va
3273
100R
3274
4K7
3278
150R
3277
4K7
F222
F223
7170
TCDT1103G
2275
33n
3275
10K
7275
KA431LZ
2170
2n2
3276
4K7
0227
HEATSINK


0209
TWG
+3.3V
PC_5V
+5V
-5V
AC_CLK
F241 F242
+12V
+6V
+32V
A8/9 CN7001

4. PCB CONNECTION DIAGRAM

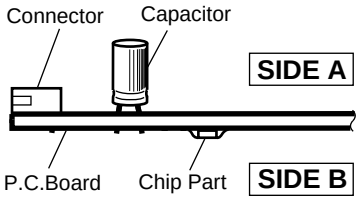
4.1 FRONT ASSY

NOTE FOR PCB DIAGRAMS :

1. Part numbers in PCB diagrams match those in the schematic diagrams.
2. A comparison between the main parts of PCB and schematic diagrams is shown below.

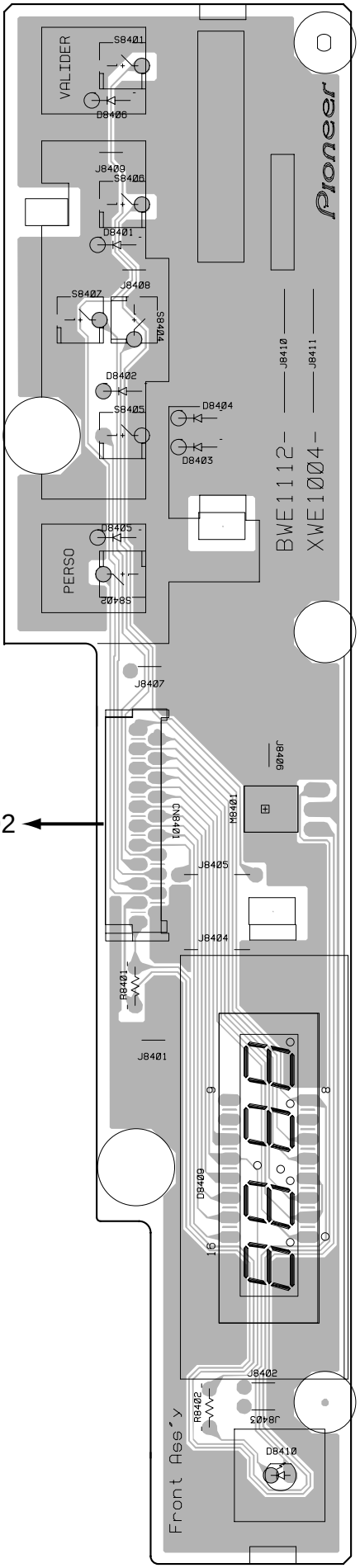
Symbol In PCB Diagrams	Symbol In Schematic Diagrams	Part Name
B C E	B C E B C E	Transistor
B C E	B C E B C E	Transistor with resistor
D G S	D G S D G S	Field effect transistor
		Resistor array
		3-terminal regulator

3. The parts mounted on this PCB include all necessary parts for several destinations.
   For further information for respective destinations, be sure to check with the schematic diagram.
4. View point of PCB diagrams.



B FRONT ASSY

SIDE A



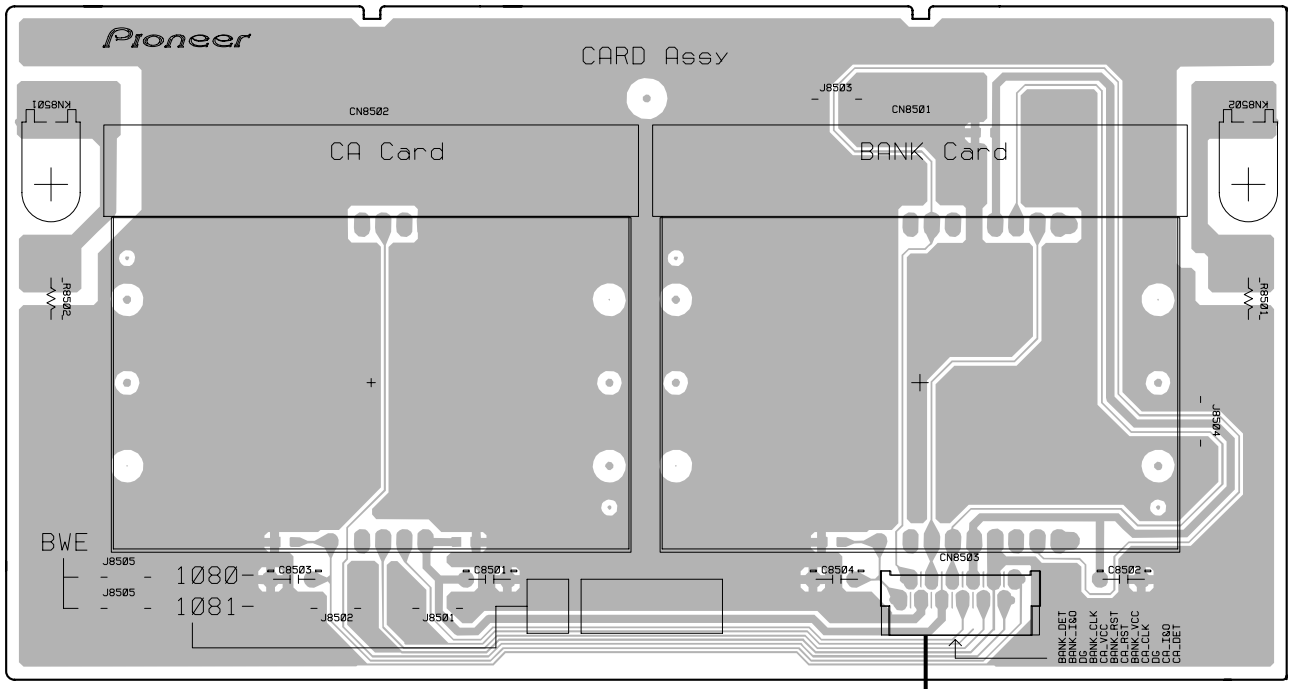
A CN7002

(XNP1008-A)

4.2 CARD ASSY

C CARD ASSY

SIDE A

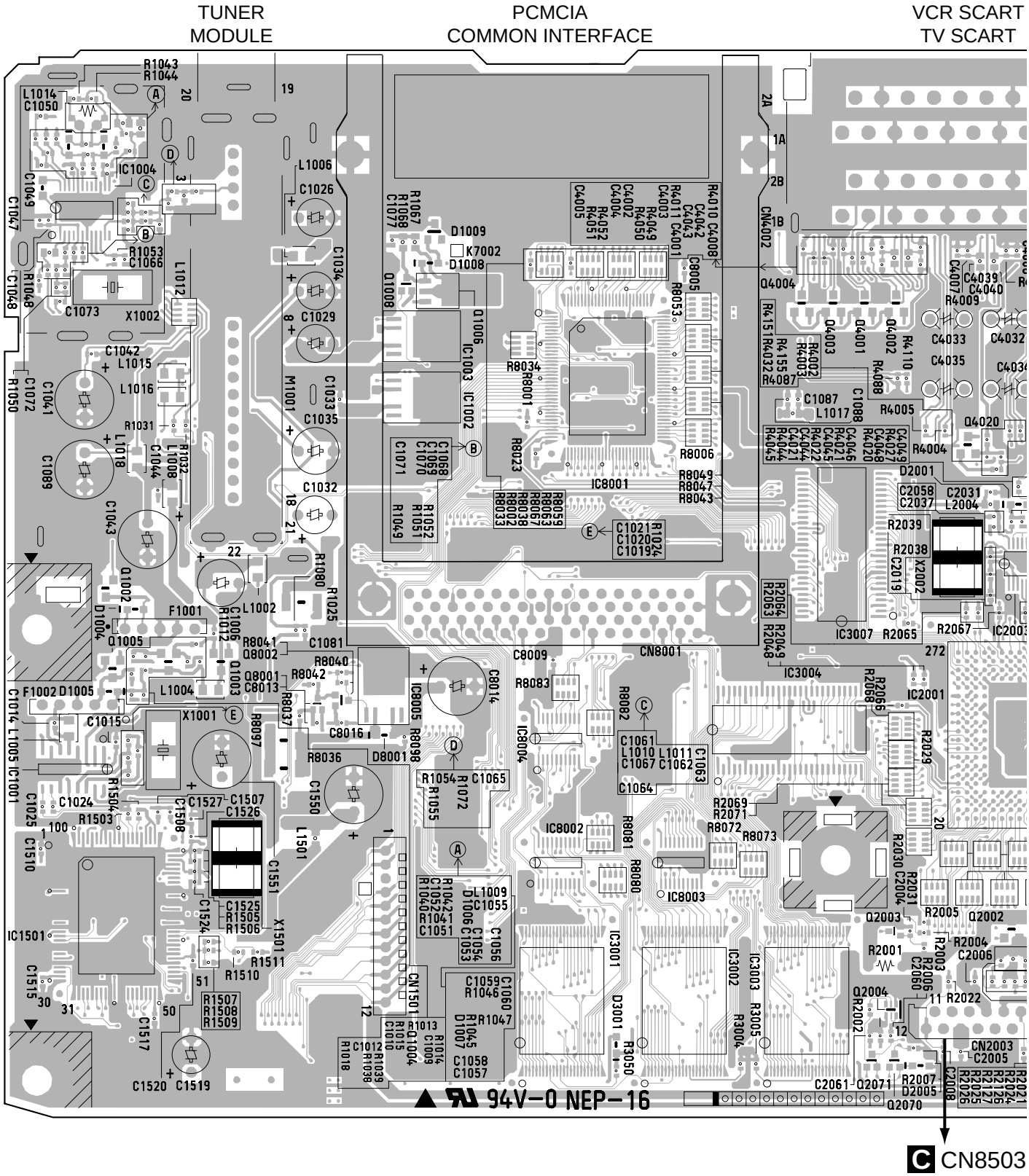


(BNP1335-C)

A CN2003

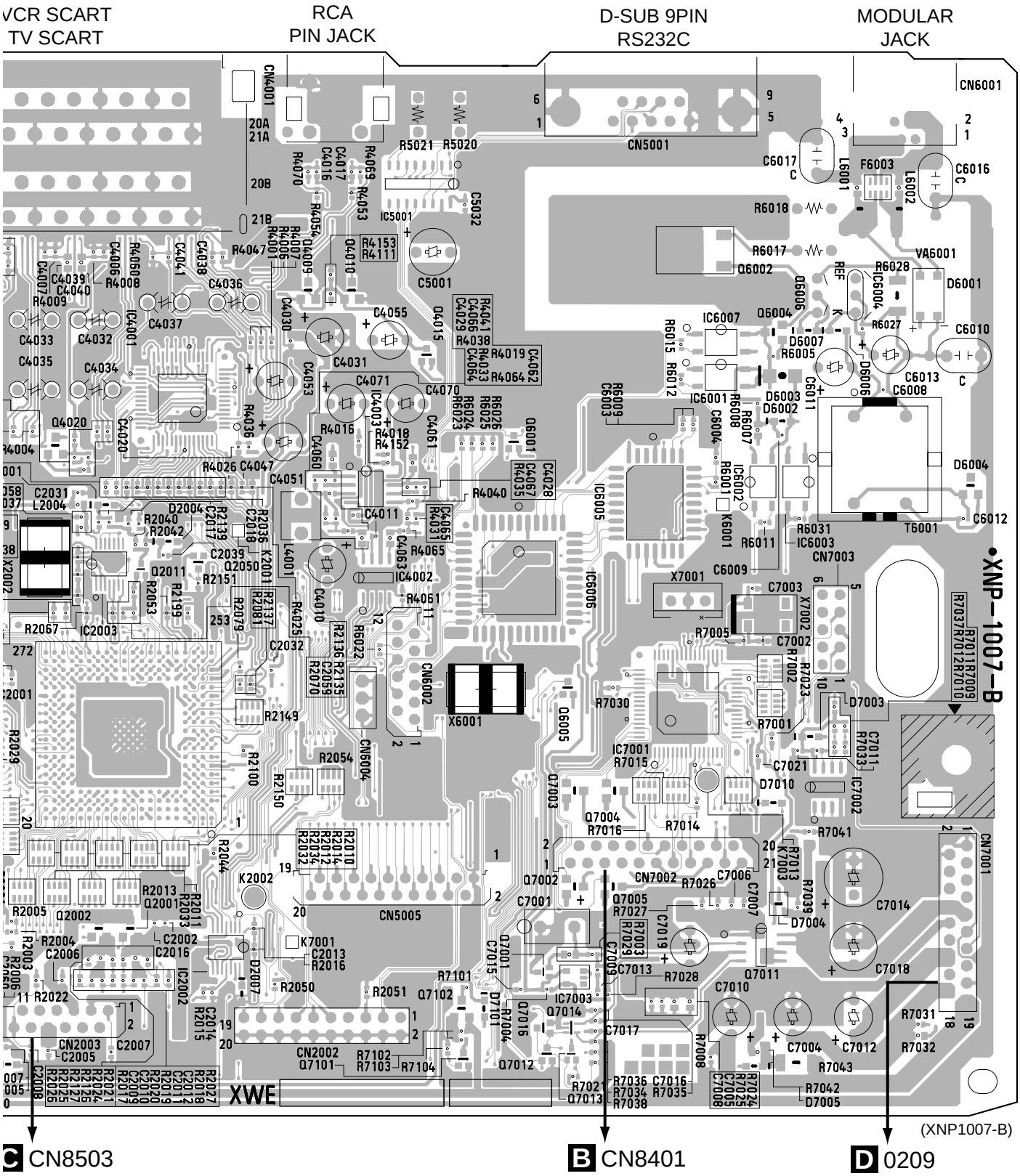
4.3 MAIN ASSY

A MAIN ASSY

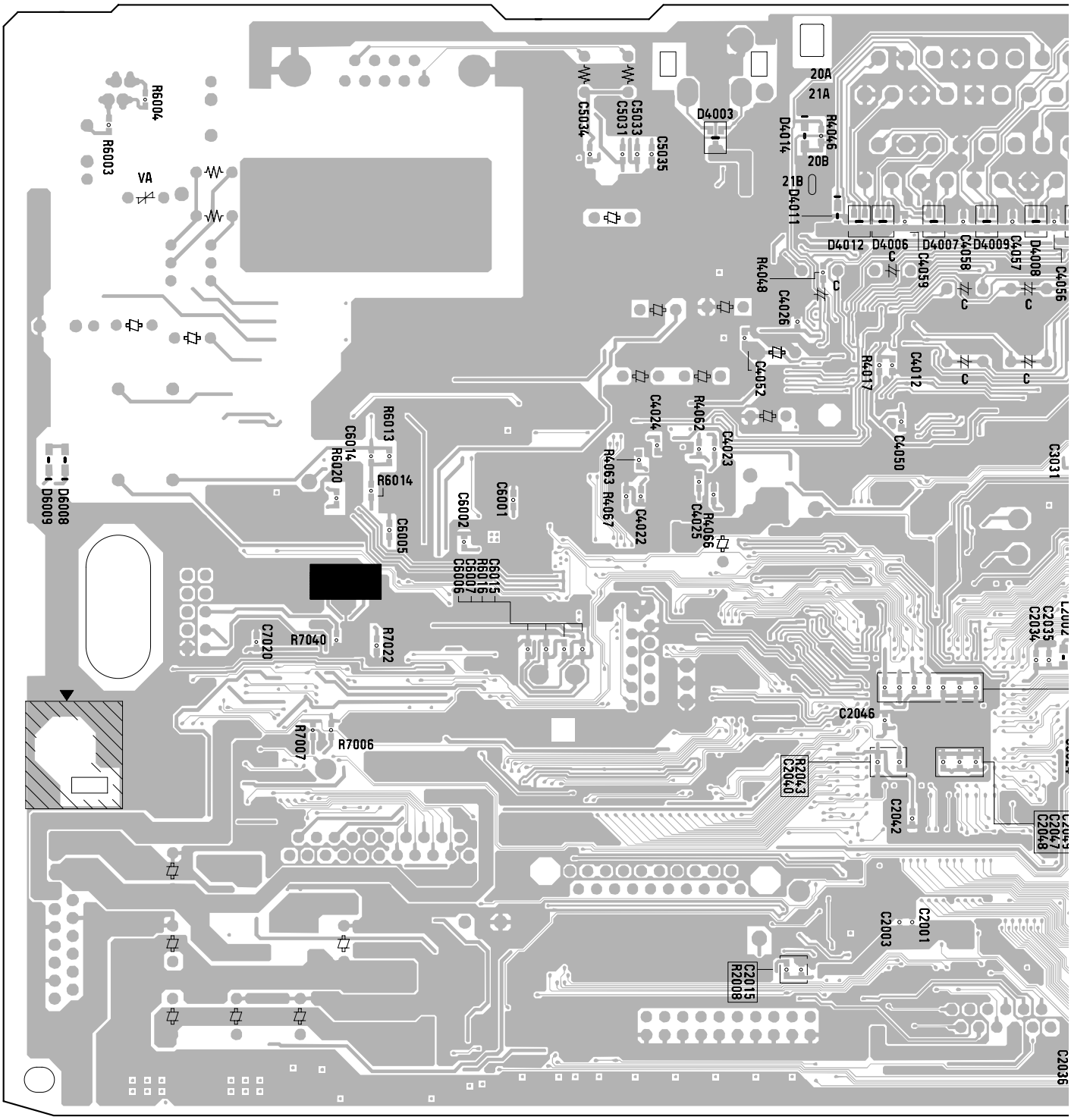


IC1004 Q1008 Q1006 Q4004 Q4003 Q4001 Q4002
Q1008 IC1003 IC1002 IC8001 Q4020
Q1005 Q1002 Q1003 Q8002 Q8001 IC8005 IC8004 IC3004 IC3007 IC2001 IC2
IC1001 IC8002 IC8003
IC1501 Q2003 Q2002
Q1004 IC3001 IC3002 IC3003 Q2071 Q2070 IC

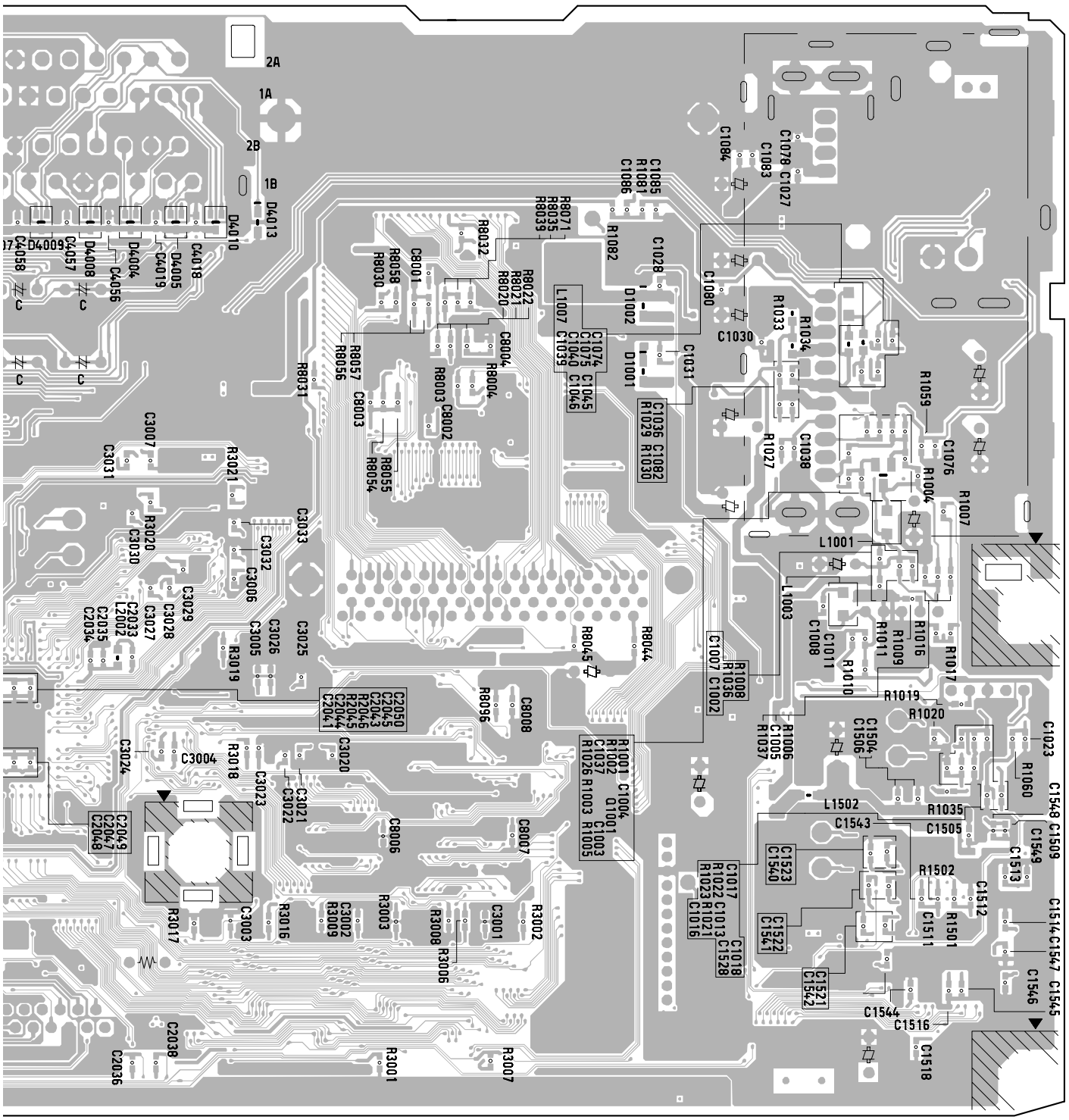
SIDE A


VCR SCART
TV SCART
RCA
PIN JACK
D-SUB 9PIN
RS232C
MODULAR
JACK
CN4001
CN5001
CN6001
C5001
IC5001
IC6001
IC6002
IC6003
IC6004
IC6005
IC6006
IC6007
IC7001
IC7002
IC7003
Q4009
Q4020
Q4015
Q6001
Q6002
Q6004
Q6006
Q7001
Q7002
Q7003
Q7005
Q7011
Q7101
Q7102
Q7012
Q7016
Q7014
Q7013
Q2001
Q2002
Q2011
Q2050
Q2070
IC2001
IC2002
IC2003
IC4002
IC4003
Q4015
Q6001
XNP−1007−B
(XNP1007-B)
C CN8503
B CN8401
D 0209

A MAIN ASSY


R6004
R6003
VA
C5034
C5033
C5031
C5035
D4003
D4014
R4046
20A
21A
20B
21B
D4011
D4012
D4006
D4007
D4009
C4057
C4058
C4059
D4008
C4056
R4048
C4026
C4052
R4017
C4012
C4024
R4062
C4023
C4050
C3031
R6013
C6014
R6020
R6014
C6005
C6002
C6001
R4063
R4067
C4022
C4025
R4066
D6008
D6009
C6013
R6016
C6007
C6006
C7020
R7040
R7022
R7007
R7006
C2046
R2043
C2040
C2042
C2035
C2034
C2047
C2048
C2003
C2001
C2015
R2008
C2036

SIDE B



(XNP1007-B)

5. PCB PARTS LIST

NOTES: ●*Parts marked by "NSP" are generally unavailable because they are not in our Master Spare Parts List.*
●*The ⚠ mark found on some component parts indicates the importance of the safety factor of the part. Therefore, when replacing, be sure to use parts of identical designation.*
●*When ordering resistors, first convert resistance values into code form as shown in the following examples.*
Ex.1 When there are 2 effective digits (any digit apart from 0), such as 560 ohm and 47k ohm (tolerance is shown by J=5%, and K=10%).
560 Ω → 56 × 10¹ → 561 ..... RD1/4PU 5 6 1 J
47k Ω → 47 × 10³ → 473 ..... RD1/4PU 4 7 3 J
0.5 Ω → R50 ..... RN2H R 5 0 K
1 Ω → 1R0 ..... RS1P 1 R 0 K
Ex.2 When there are 3 effective digits (such as in high precision metal film resistors).
5.62k Ω → 562 × 10¹ → 5621 ..... RN1/4PC 5 6 2 1 F

Mark	No.	Description	Part No.
LIST OF ASSEMBLIES			
	MAIN ASSY		XWE1003
	FRONT ASSY		XWE1004
	CARD ASSY		XWE1006
⚠	POWER ASSY		XXF1002
A MAIN ASSY			
SEMICONDUCTORS			
	IC8001		103563
	IC6005		73K324BL-IH
	IC8003		74LCX245MTCX
	IC8002,IC8004		74LCX373MTCX
	IC2003		74LVU04PW
	IC6006		AMC2442ACVF(0.84)
	IC1002,IC8005		BA05SFP
	IC7002		CAT24WC64J
	IC4002		CS4335-KS
	IC4001		CXA2161R
	IC5001		HIN202CBN
	IC3004,IC3007		HYB39S64160BT-8
	IC4003		NJM4558MD
	IC7001		PE5181A
	IC7003		PST9124N
	IC2002		SN74ACT08PWR
	IC1501		SQC6100
	IC2001		STI5512MWE
	IC1004		TA1297AFN
	IC1001		TDA6190X
	IC3001		XGC1001-A-AV
	IC3002		XGC1002-A-AV
	IC3003		TC58FVT160FT-85
⚠	IC6001		TLP127
⚠	IC6007		TLP181(GR)
	Q7102		2SA1036K
	Q2003,Q7001,Q8001		2SA1576A
	Q2001		2SC2411K
	Q4020		2SC2412K
	Q2011,Q6004,Q7013		2SC4081
	Q1006		2SD1664
	Q6002		2SD1760
	Q1001,Q1003,Q1004		BF799
	Q2050,Q2071,Q6001		DTA124EUA
	Q4015		DTA143EUA
	Q7002-Q7005		DTB113ZK
	Q4001,Q4002,Q4009,Q4010		DTC123TKA
	Q1008,Q7012,Q7016,Q8002		DTC124EUA
	Q7101		DTC143EUA
	Q6005		DTC144TUA
	Q7011		TPC8201
	Q2004		UMD2N
	Q7014		UMG1N
	D1001,D3001,D7003,D7010,D8001		1SS355
	D1009		BAS70
	D1006,D1007		BB639C
	D7004		DAP202U
	D2001		HVU356
	D4013,D4014,D7101		PDZ12B
	D7005		PDZ4.7B
	D2005		PDZ5.6B
	D2004		PDZ8.2B
	D6003		PTZ43A
	D6001		S1ZB60-4072
	D6008,D6009		UDZ4.3B
	D1008		UDZS9.1B
	D4003-D4010,D4012		UMZ12N
⚠	VA6001		2322 594 51516
COILS AND FILTERS			
	F6003	CHIP INPEDER ARRAY	BTF1087
	L4001	RADIAL INDUCTOR	BTH1065
	L2002,L2004	CHIP INPEDER	DTL1038
	L1015,L1016		LCYA3R3J2520
	F1001,F1002	CHIP INDUCTOR (1μH)	XTF1001
	L1001,L1002,L1004,L1007	CHIP INDUCTOR (1μH)	XTL1001
	L1501,L1502	CHIP INDUCTOR (1μH)	XTL1001
	L1011	CHIP INDUCTOR (8.2nH)	XTL1002
	L1006,L1017	CHIP FERRITE BEAD	XTL1006
	L1008,L1018	CHIP INDUCTOR (10μH)	XTL1007
	L1010	CHIP INDUCTOR (6.8nH)	XTL1009
	L1012	CHIP BEAD ARRAY	XTL1010
	L1014	CHIP INDUCTOR (15nH)	XTL1011

Mark	No.	Description	Part No.
TRANSFORMER			
⚠	T6001	LINE TRANS.	BTX1035
CAPACITORS			
	C7001 (0.047F/5.5V)		ACH1246
⚠	C6016,C6017 (470pF/12kV)		BCG1026
	C1037,C1038,C1045,C1046		CCSRCH100D50
	C1511,C1512		CCSRCH100D50
	C1065,C1067,C4022,C4023		CCSRCH101J50
	C1084		CCSRCH121J50
	C1524,C1526		CCSRCH150J50
	C1083		CCSRCH180J50
	C7002,C7003		CCSRCH220J50
	C1030,C1033,C1036,C1047,C1527		CCSRCH221J50
	C2005,C2007,C2013,C2018		CCSRCH221J50
	C4028,C4029		CCSRCH221J50
	C2011,C2012,C2019		CCSRCH330J50
	C1074,C1076		CCSRCH331J50
	C1078,C1080-C1082,C1085-C1088		CCSRCH390J50
	C1540-C1549,C3020-C3033		CCSRCH390J50
	C6006,C6007		CCSRCH390J50
	C1075		CCSRCH471J50
	C1055		CCSRCH4R7C50
	C1061		CCSRCH5R0C50
	C1053,C1054,C1056,C1069		CCSRCH680J50
	C1068		CCSRCH7R0D50
	C1063		CCSRCJ3R0C50
	C1062,C1064		CCSRCKR50C50
	C4031,C4051,C4053,C6013,C7010		CEAK100M50
	C4070,C4071,C7004,C7019		CEAK101M10
	C5001		CEAK101M25
	C1041		CEAK101M50
	C7018		CEAK221M10
	C1006		CEAK221M25
	C6011		CEAK3R3M50
	C4010,C8014		CEAK470M16
	C1026,C1029,C1032,C1034,C1519		CEAK470M25
	C7012		CEAK470M25
	C1043,C1089,C1550,C1551,C7014		CEAK471M10
	C4055		CEAK4R7M50
	C4036,C4037		CEANP100M50
	C1049,C1071,C4039,C4040		CKSQYB105K10
	C4042,C4043,C4060-C4063		CKSQYB105K10
	C1060		CKSQYB473K50
	C1039,C1040,C1059		CKSQYF104Z50
	C1018,C1020,C1066,C2034,C2038		CKSRYB102K50
	C2058,C4001-C4008,C4016,C4017		CKSRYB102K50
	C6002		CKSRYB102K50
	C1003-C1005,C1009,C1010,C1012		CKSRYB103K50
	C1015,C1024,C1025,C1051,C1052		CKSRYB103K50
	C1058,C1507,C2031,C2033,C2035		CKSRYB103K50
	C2037,C2060,C4011,C4024,C4025		CKSRYB103K50
	C8013,C8016		CKSRYB103K50
	C4038,C4041,C4044-C4049		CKSRYB104K16
	C1057		CKSRYB222K50
	C6008		CKSRYB273K16
	C6012		CKSRYB333K25
	C2059,C2061,C7007,C7008		CKSRYB471K50
	C7016,C7017		CKSRYB473K16
	C1002,C1007,C1011,C1013		CKSRYF104Z16
	C1016,C1017,C1023,C1027,C1028		CKSRYF104Z16
	C1031,C1044,C1048,C1050,C1070		CKSRYF104Z16
	C1072,C1073,C1077,C1504-C1506		CKSRYF104Z16
	C1508-C1510,C1513-C1518		CKSRYF104Z16
	C1520-C1523,C2004,C2015,C2032		CKSRYF104Z16
	C2039-C2050,C3001-C3007,C4012		CKSRYF104Z16
	C4018-C4021,C4026,C4030,C4050		CKSRYF104Z16
	C4052,C4056-C4059,C5031-C5035		CKSRYF104Z16
	C6001,C6003-C6005,C7005,C7006		CKSRYF104Z16
	C7009,C7011,C7013,C7015		CKSRYF104Z16
	C7020,C7021,C8001-C8009		CKSRYF104Z16
	C2002		CKSRYF224Z16
	C2017		CKSRYF474Z16
RESISTORS			
	R2150,R7001,R7013		RAB4C102J
	R2010,R2054,R2149,R8034		RAB4C103J
	R7015,R7016		RAB4C181J
	R2011-R2014,R2029-R2034		RAB4C220J
	R2068,R2069,R2071		RAB4C220J
	R7002		RAB4C333J
	R8002,R8006,R8043,R8047,R8049		RAB4C470J
	R8053,R8059,R8063,R8067		RAB4C470J
	R8072,R8073,R8080-R8083		RAB4C470J
	R2001		RD1/2VM3R3J
	R1034,R8054,R8056		RS1/10S0R0J
	R2024,R2025,R7024,R7025,R7029		RS1/10S471J
	R1067,R1068		RS1/10S561J
	R7042		RS1/10S681J
	R4020-R4022,R4025-R4027		RS1/16S2000F
	R6028		RS1/2S180J
	R1025,R8036,R8097		RS1/2S1R5J
	Other Resistors		RS1/16S□□□J
OTHERS			
	CN2003	12P FFC CONNECTOR	9604S-12C
	CN7002	21P FFC CONNECTOR	9604S-21C
	JA4001	2P PIN JACK	BKB1017
	CN4002	DUAL SCRAT CONNECTOR	BKN1019
	CN7001	19P PLUG	BKP1120
	CN5001	D-SUB 9P CONNECTOR	BKP1122
⚠	CN6001	4P MODULAR JACK	BKP1137
	X2002	CRYSTAL RESONATOR (27MHz)	BSS1061
	X7002	CRYSTAL RESONATOR (32.768kHz)	BSS1091
	X7001	CERALOCK (8.0MHz)	BSS1097
	X6001	X'TAL (11.0592MHz)	BSS1099
	CN8001	PCMCIA CONNECTOR	XKP1001
	X1002	X'TAL (4MHz)	XSS1002
	X1501	X'TAL (28.9MHz)	XSS1003
	M1001	TUNER MODULE	XXF1001
	M1004	TUNER SHIELD	XNB1003
	M1005	TUNER BOTTOM CAN	XNB1004

B FRONT ASSY

SEMICONDUCTOR		
	D8409	BEL1037
SWITCHES		
	S8401,S8402,S8404-S8407	ASG7013

Mark	No.	Description	Part No.

RESISTOR

	R8401 (27kΩ)	BCN1056

OTHERS

CN8401	21P FFC CONNECTOR	9607S-21F
J8420	21P FLEXIBLE FLAT CABLE	BDD1042
M8401	REMOTE RECEIVER UNIT	BXX1034

C CARD ASSY

CAPACITORS

	C8501-C8504	CKCYF103Z50

RESISTORS

	All Resistors	RD1/4PU□□□J

OTHERS

CN8503	12P CONNECTOR (L)	9604S-12F
CN8502	8P CARD CONNECTOR	BKP1141

D POWER ASSY

POWER ASSY has no service part as a assy part. Only the fuse(0109:REK1102) is the service part as a set part. Refer to page 5.

6. ADJUSTMENT

There is no information to be shown in this chapter.

7. GENERAL INFORMATION

7.1 IC

• The information shown in the list is basic information and may not correspond exactly to that shown in the schematic diagrams.

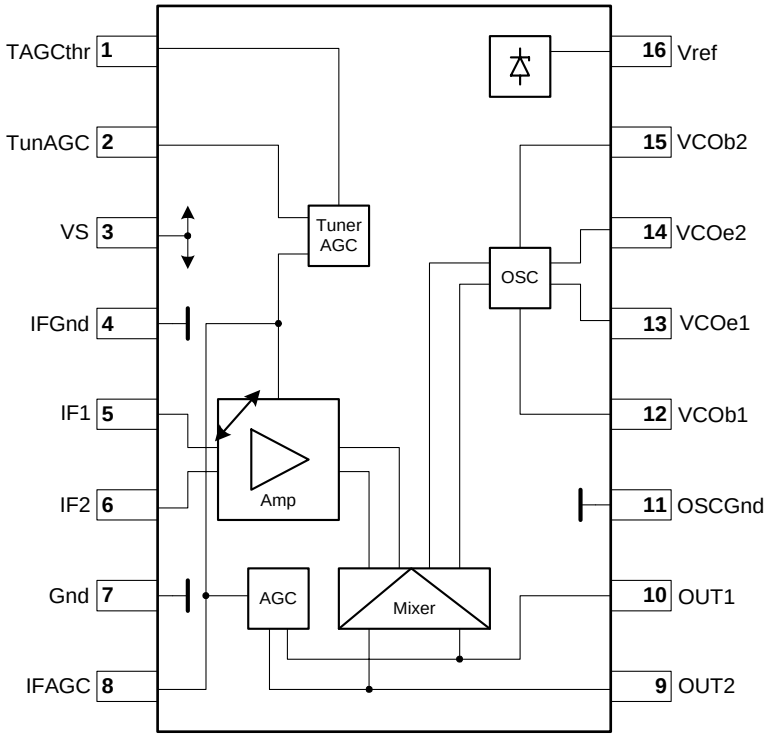
●List of IC

TDA6190X, TA1297AFN, SQC6100, STI5512MWE, CXA2161R, CS4335-KS, HIN202CBN, 73K324BL-IH, AMC2442ACV(0.84), PE5181A

■ TDA6190X (MAIN ASSY : IC1001)

• TV IF IC

● Block Diagram



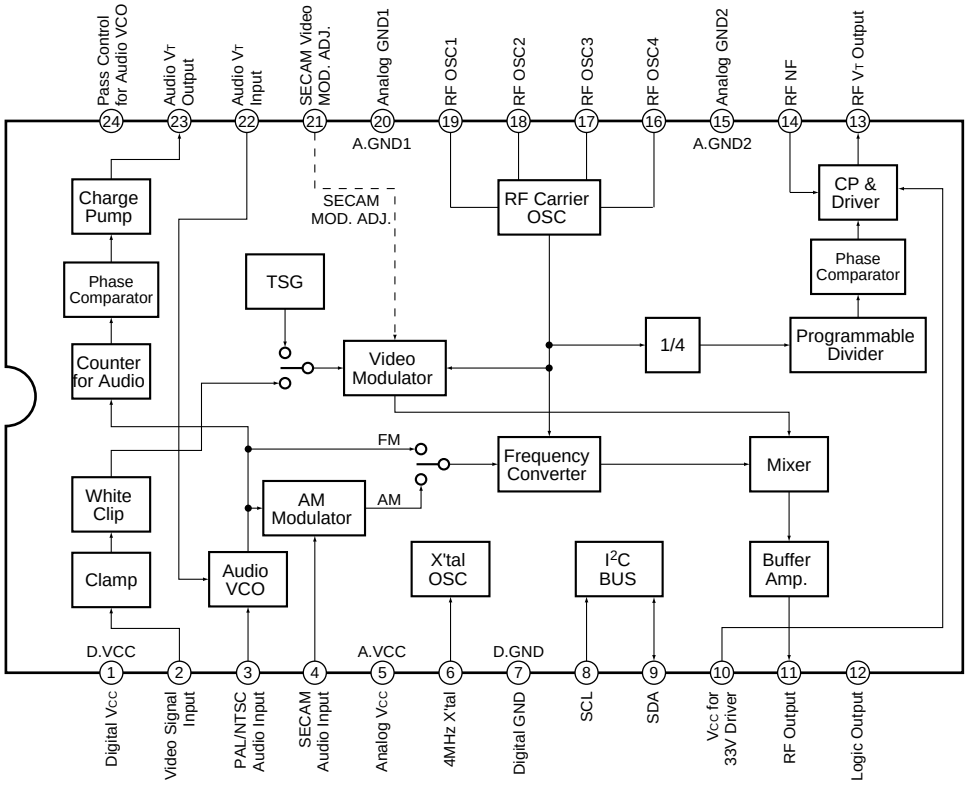
● Pin Function

No.	Pin Name	Function
1	TAGCthr	Tuner AGC threshold; delayed tuner AGC adjust input ; if not required,connect to reference voltage Vref
2	TunAGC	Delayed Tuner AGC output; open NPN transistor collector
3	Vs	Supply voltage
4	IFGnd	IF input Ground
5	IF1	IF input IF1; balanced to IF2
6	IF2	IF input IF2; balanced to IF1
7	Gnd	Ground
8	IFAGC	IF AGC filter; automatic gain control filter pin, low voltage corresponds to maximum gain
9	OUT2	Buffered mixer output OUT2; balanced to OUT1
10	OUT1	Buffered mixer output OUT1; balanced to OUT2
11	OSCGnd	Oscillator Ground
12	VCOb1	VCO base 1; balanced to VCOb2
13	VCOe1	VCO emitter 1; balanced to VCOe2
14	VCOe2	VCO emitter 2; balanced to VCOe1
15	VCOb2	VCO base 2; balanced to VCOb1
16	Vref	Reference voltage

TA1297AFN (MAIN ASSY : IC1004)

- **Modulator IC**

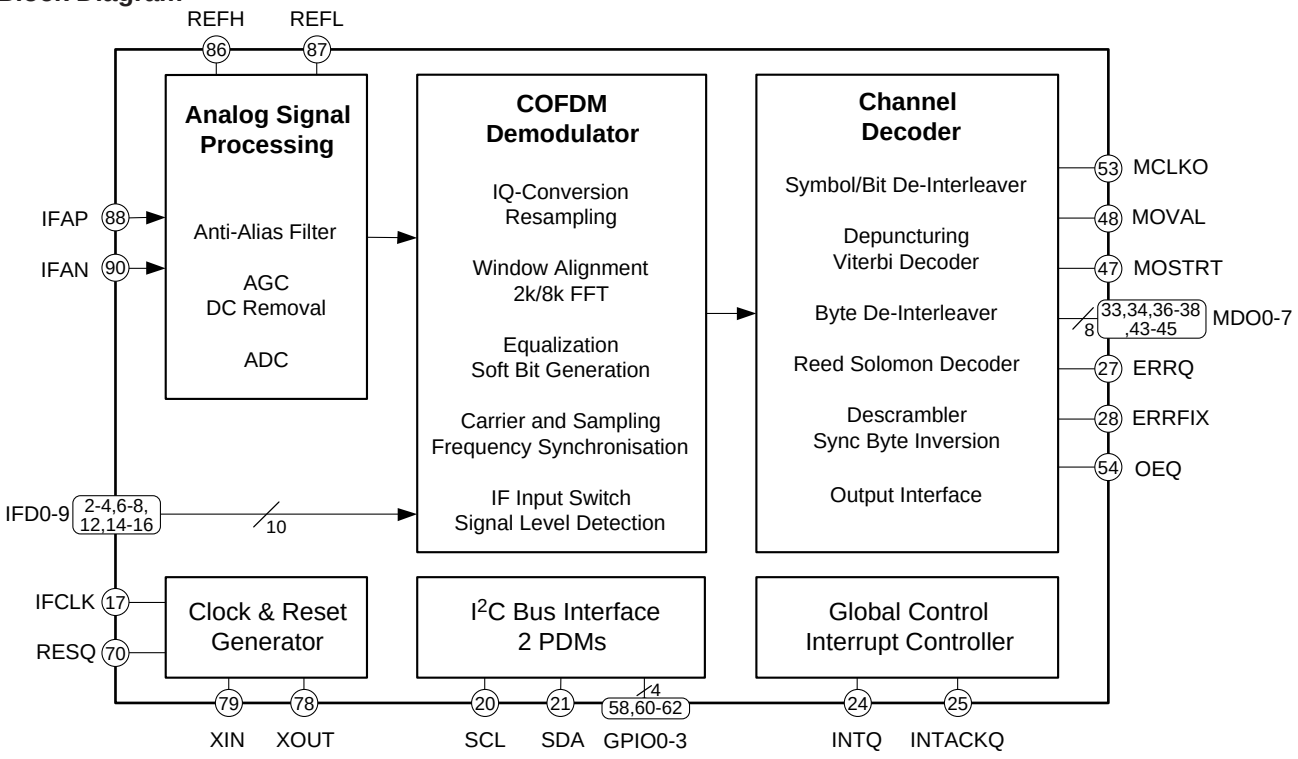
● **Block Diagram**



SQC6100 (MAIN ASSY : IC1501)

- **COFDM Demodulator IC**

● **Block Diagram**



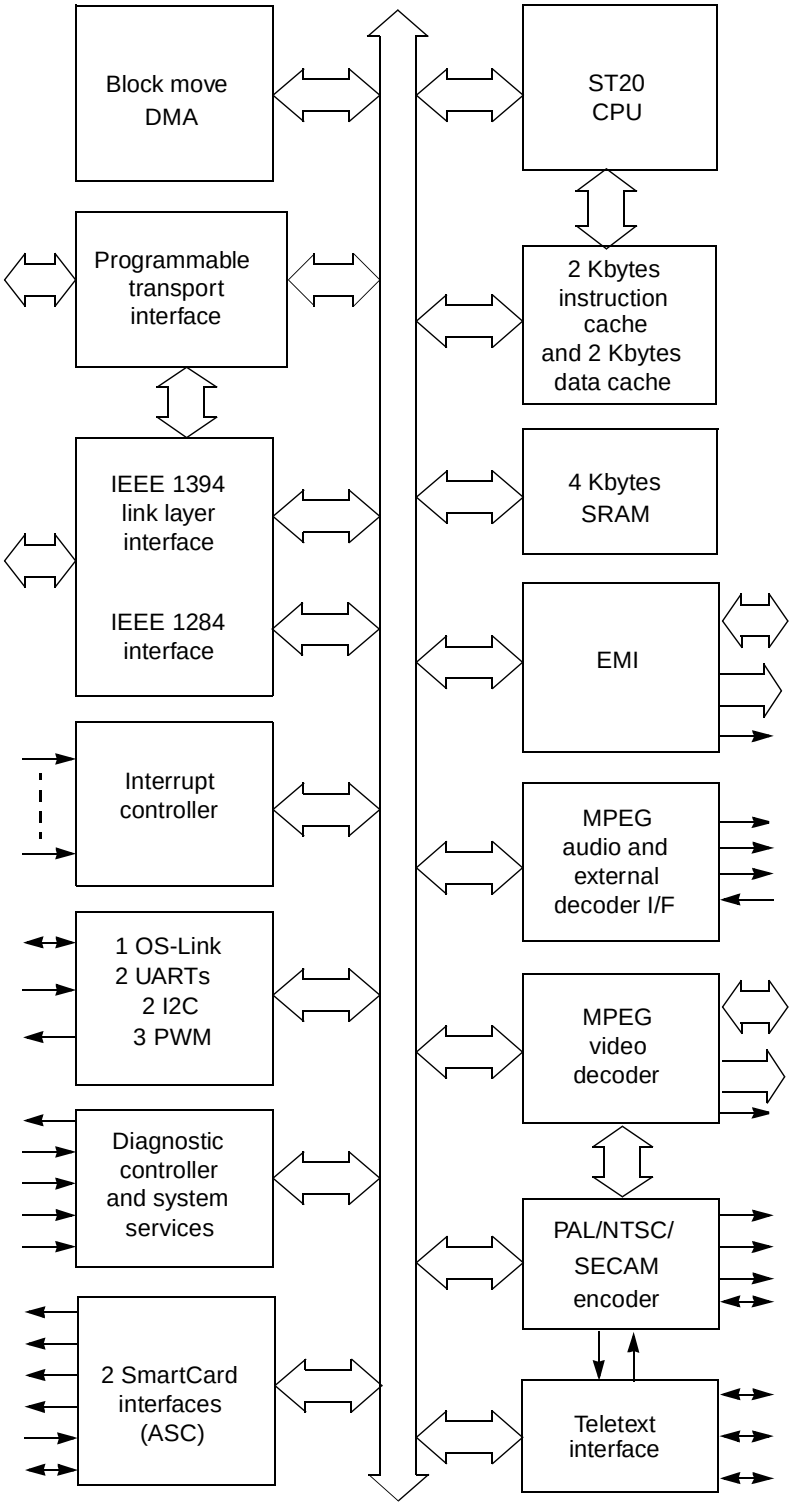
● Pin Function

No.	Name	I/O	Function	No.	Name	I/O	Function
1	VSSD	–	Digital ground	51	VSSD	–	Digital ground
2	IFD0	I	Digital IF input bit 0 (LSB)	52	VSSD	–	Digital ground
3	IFD1		Digital IF input bit 1	53	MCLKO	O	Clock for output TS data
4	IFD2		Digital IF input bit 2	54	OEQ	I	Output enable
5	VSSD	–	Digital ground	55	VSSD	–	Digital ground
6	IFD3	I	Digital IF input bit 3	56	VDDD	–	3.3V digital power supply
7	IFD4		Digital IF input bit 4	57	VSSD	–	Digital ground
8	IFD5		Digital IF input bit 5	58	GPIO0	I/O	General purpose digital input/output port 0
9	VSSD	–	Digital ground	59	VSSD	–	Digital ground
10	VDDD	–	3.3V digital power supply	60	GPIO1	I/O	General purpose digital input/output port 1
11	VSSD	–	Digital ground	61	GPIO2	I/O	General purpose digital input/output port 2
12	IFD6	I	Digital IF input bit 6	62	GPIO3	I/O	General purpose digital input/output port 3
13	VSSD	–	Digital ground	63	VSSD	–	Digital ground
14	IFD7	I	Digital IF input bit 7	64	VDDD	–	3.3V digital power supply
15	IFD8		Digital IF input bit 8	65	VSSD	–	Digital ground
16	IFD9		Digital IF input bit 9 (MSB)	66	VSSD	–	Digital ground
17	IFCLK	O	Clock for external IF ADC	67	VDDD	–	3.3V digital power supply
18	VSSD	–	Digital ground	68	VSSD	–	Digital ground
19	VDDD	–	3.3V digital power supply	69	VSSD	–	Digital ground
20	SCL	I	Serial clock line	70	RESQ	I	System reset
21	SDA	I/O	Serial data line	71	VSSD	–	Digital ground
22	VSSD	–	Digital ground	72	VSSD	–	Digital ground
23	VSSD	–	Digital ground	73	NC	–	No connection
24	INTQ	O	Interrupt request	74	NC	–	No connection
25	INTACKQ	I	Interrupt acknowledge	75	VDDD	–	3.3V digital power supply
26	VSSD	–	Digital ground	76	VSSD	–	Digital ground
27	ERRQ	O	Erroneous frame on data output TS	77	VSSD	–	Digital ground
28	ERRFIX	O	Error fixed data on data output TS	78	XOUT	O	Output for crystal oscillator
29	VDDD	–	3.3V digital power supply	79	XIN	I	Input for external clock or crystal oscillator
30	VSSD	–	Digital ground	80	VSSD	–	Digital ground
31	VSSD	–	Digital ground	81	VSSD	–	Digital ground
32	VSSD	–	Digital ground	82	VDDA	–	3.3V analog power supply
33	MDO0	O	TS data output bit 0 (LSB)	83	VSSA	–	Analog ground
34	MDO1		TS data output bit 1	84	VDDA	–	3.3V analog power supply
35	VSSD	–	Digital ground	85	VSSD	–	Digital ground
36	MDO2	O	TS data output bit 2	86	REFH	–	High reference voltage for ADC
37	MDO3		TS data output bit 3	87	REFL	–	Low reference voltage for ADC
38	MDO4		TS data output bit 4	88	IFAP	I	Positive analog IF input
39	VSSD	–	Digital ground	89	VSSD	-	Digital ground
40	VDDD	–	3.3V digital power supply	90	IFAN	I	Negative analog IF input
41	VSSD	–	Digital ground	91	VSSA	–	Analog ground
42	VSSD	–	Digital ground	92	VSSD	–	Digital ground
43	MDO5	O	TS data output bit 5	93	VSSA	–	Analog ground
44	MDO6		TS data output bit 6	94	VSSA	–	Analog ground
45	MDO7		TS data output bit 7 (MSB)	95	NC	–	No connection
46	VSSD	–	Digital ground	96	VSSD	–	Digital ground
47	MOSTRT	O	Frame start byte on data output TS	97	VDDA	–	3.3V analog power supply
48	MOVAL	O	Data valid signal for data output TS	98	VSSD	–	Digital ground
49	VDDD	–	3.3V digital power supply	99	VDDD	–	3.3V digital power supply
50	VSSD	–	Digital ground	100	VSSD	–	Digital ground

STI5512MWE (MAIN ASSY : IC2001)

- **Programmable Transport IC**

- **Block Diagram**



- **Pin Function (1/5)**

Signal names are prefixed by **not** if they are active low; otherwise they are active high.

Pin	Number	Function
VDD	13	Power supply
GND	16	Ground
VClamp1-3[1]	3	Power supply for clamp diodes
VDDA0-1	2	Analog power supply for PAL/NTSC/SECAM encoder
VSSA0-1	2	Analog ground for PAL/NTSC/SECAM encoder
RTCVDD	1	Real time clock supply
VDD_VPLL	1	Analog power supply for video PLL
VSS_VPLL	1	Analog ground for video PLL

Table 1 Power supply pins

1. The VClamp pins are a power supply bus used to diode clamp the voltage on 5V tolerant digital input or output pins to. The voltage on the digital signal pin is then clamped to within VImax (5.5V) if the applied voltage is increased above 5V.

   If the device is to be interfaced to 3.3V logic signals only, then the VClamp pins can be connected to the STi5512 3.3V VDD power supply. However if any pin is to be interfaced to a 5V logic signal, then the VClamp pins must be connected to the 5V power supply (the 5V logic device power supply). Note in this case the 5V power supply must be capable of sinking the clamp current of transient signals above 5V.

   In the latter case it is important to ensure the correct power supply ramp sequence. The VClamp power supply must be applied before or at the same time as the VDD 3.3V power supply. This is to ensure that during power supply power up and power down, VClamp > VDD + 0.5V.

Pin	In/Out	Function
R_OUT[1]	out	Red output
G_OUT[1]	out	Green output
B_OUT2[1]	out	Blue output
C_OUT[1]	out	Chroma output
CV_OUT[1]	out	Composite video output
Y_OUT[1]	out	Luma output
I_REF_DAC_RGB[1]	in	DAC current reference
I_REF_DAC_YCC[1]	in	DAC current reference
V_REF_DAC_RGB[1]	in	DAC voltage reference
V_REF_DAC_YCC[1]	in	DAC voltage reference
OSD_ENABLE	in/out	OSD enable
notHSYNC	in/out	Horizontal sync
ODD_OR_EVEN	in/out	Vertical sync
YC0-7[2]	output	Digital YUV output
CFC	input	DENC color burst phase and frequency control. This pin can be used in non-scart based Genlock applications. If it is not used, this pin must ground.

Table 2 Video output interface pins

• Pin Function (2/5)

1. The digital encoder video outputs are analogue signals and are not 5V tolerant. The same applies to the video DAC voltage and current reference pins.

2. The **YC0** pin is tri-stated during reset and then sampled at the end of the reset to determine whether the EMI pins are in STi5510 or STi5512 mode. If the **YC0** pin is sampled high (i.e at VDD) then the STi5510 mode is selected for the EMI pins and a low value selects STi5512 mode. In STi5512 mode the address shift for bank 3 is dependent on the boot bank width and the strobe pins are tri-stated when the EMI bus is granted to an external DMA device. External 10KΩ pull-up or pull-down resistors should be fitted to the **YC0** according to the functionality desired. If this pin is left *not* connected, the pin will be pulled high by an internal pull-up and will default the EMI pins to STi5510 mode.

Pin	In/Out	Function
SCLK/A_C_STB	out	Serial clock or AC-3 data strobe
PCM_DATA/A_C_DATA	out	PCM data out or AC-3 data out
PCMCLK	in/out	PCM clock
LRCLK/A-WORD_CLK	out	Left/right clock or AC-3 word clock
notA_C_REQ i	n	AC-3 data request
notA_PTS_STB	in	AC-3 audio PTS strobe

Table 3 AC-3/MPEG1 audio output interface pins

Pin	In/Out	Function
Interrupt0-1	in	Interrupt

Table 4 External interrupt pins

Pin	In/Out	Function
ClockIn	in	System input clock - PLL or TimesOneMode
SpeedSelect0-1	in	PLL speed selector
notRST	in	System reset
CPUAnalyse / TrigIn	in	Error analysis / External trigger input to DCU
CPUReset	in	Soft reset for analyzing from OS-Link
ErrorOut / TrigOut[1]	in/out, out	Error indicator / Signal to trigger external debug circuitry (e.g. LSA)

Table 5 System services pins

1. This pin is tri-stated during reset and then sampled at the end of the reset to determine whether the OS-Link is active and to determine the function of the shared **CPUAnalyse / TrigIn** and the **ErrorOut / TrigOut**, as described in the *System Services* chapter. If the **ErrorOut** pin is sampled high (i.e at VDD) then the DCU signals (**TrigIn** and **TrigOut**) are selected and a low value indicates OS-Link signals (i.e. **CPUAnalyse**, **ErrorOut**) are to be used. External 10KΩ pull-up or pull-down resistors should be fitted to the **ErrorOut** according to the functionality desired.

• **Pin Function (3/5)**

Pin	In/Out	Function
MemAddr2-23 out		Address bus
MemData0-31	in/out	Data bus. **MemData0** is the least significant bit (LSB) and **MemData31** is the most significant bit (MSB).
MemRdnotWr out		ReadnotWrite strobe
MemReq	in	Direct memory access request
MemGrant	out	Direct memory access granted
MemWait i	n	Memory cycle extender
notMemCAS0,2	out	CAS strobes for SDRAM/DRAM in Banks 0 and 1
notMemCAS1	out	CAS strobe for DRAM or SDRAM clock
notMemCAS3	out	CAS strobe for DRAM or sub-bank chip select for bank 3
notMemRAS0	out	RAS strobe for SDRAM/DRAM in Bank 0, chip select for Bank0 or RAS strobe for lowest DRAM sub-bank in Bank0
notMemRAS1	out	RAS strobe for highest DRAM sub-bank in Bank0 or SDRAM Chip select signal for highest sub-bank of Bank0
notMemRAS2	out	RAS strobe for SDRAM/DRAM in bank 1, chip select for Bank1 or RAS strobe for lowest DRAM sub-bank in Bank1
notMemRAS3	out	RAS strobe for highest DRAM sub-bank in Bank1 or SDRAM Chip select signal for Bank1
notMemCSROM	out	Chip select strobe for ROM in bank3.
notSDRAMCS0	out	SDRAM Chip select signal for Bank0 or lowest sub-bank of Bank0
notMemOE	out	Output enable strobe - banks 0-3.
notMemBE0-3	out	Byte enable strobes - banks 0-3.
notMemCS2	out	Chip select strobe for memory in bank 2.
BootSource0-1	in	Boot from ROM or from link.
ProcClockOut	out	Processor clock.

Table 6 STi5512 External memory interface pins

Pin	In/Out	Function
AD0-12 out		SDRAM address bus
DQ0-15	in/out	SDRAM data bus (lower byte)
notSDCS0	out	SDRAM chip select for first SDRAM
notSDCS1/AD13	out	SDRAM chip select for second SDRAM or AD13
notSDCAS out		SDRAM CAS
notSDRAS out		SDRAM RAS
notSDWE out		SDRAM write enable
MEMCLKIN	in	SDRAM memory clock input
MEMCLKOUT	out	SDRAM memory clock output
DQML	out	DQ mask enable (lower)
DQMU	out	DQ mask enable (upper)

Table 7 Shared SDRAM interface pins

• **Pin Function (4/5)**

Pin	In/Out	Function
LPClockIn[1]	in	Low power input clock
LPClockOsc[1]	in/out	Low power clock oscillator
AUX_CLK_OUT	out	Auxiliary clock for general use

Table 8 Low power controller and real time clock pins

1. The low power clock pins are not 5V tolerant.

Pin	In/Out	Function
PIO0[0-7]	in/out	Parallel input/output pin or alternative function (see Table 15)
PIO1[0-7]	in/out	Parallel input/output pin or alternative function (see Table 15)
PIO2[0-7]	in/out	Parallel input/output pin or alternative function (see Table 15)
PIO3[0-7]	in/out	Parallel input/output pin or alternative function (see Table 15)
PIO4[0-7]	in/out	Parallel input/output pin or alternative function (see Table 15)

Table 9 PIO pins

Pin	In/Out	Function
LinkIn	in	Serial data input channel
LinkOut	out	Serial data output channel

Table 10 OS-Link pins

Pin	In/Out	Function
TSInByteClk	in	Link IC byte clock
TSInByteClkValid	in	Link IC byte clock valid edge
TSInData0-7	in	Link IC data
TSInError	in	Link IC packet error
TSInPacketClk	in	Link IC packet strobe

Table 11 Transport stream input pins

Pin	In/Out	Function
TtxtEvennotOdd	in	Teletext even not odd vertical sync signal
TtxtHsync	in	The HSYNC signal input when the teletext interface is operating in the input mode

Table 12 Teletext interface

- **Pin Function (5/5)**

The teletext clock and data inputs are shared PIO pins, as shown in Table 15 .

High speed data port pins have a dual function, and can be used either to interface to an external IEEE 1394 link layer controller or provide an IEEE 1284 parallel port interface.

Pin	In/Out	Function
1284Data0-7 / AVData0-7	in/out	IEEE 1284 port data or AV data
1284notSelectIn	in	IEEE 1284 port control signals or AV signals
1284notInit / AVPacketTag3	in	
1284notFault / AVPacketTag2	out	
1284notAutoFd / AVPacketTag1	in	
1284Select / AVPacketTag0	out	
1284PError / AVByteClkValid	out, in/out	
1284Busy / AVPacketClk	out, in/out	
1284notAck / AVByteClk	out	
1284notStrobe/AVPacketError	in	

Table 13 High-speed data port pins

Pin	In/Out	Function
TDI	in	Test data input
TDO	out	Test data output
TMS	in	Test mode select
TCK	in	Test clock
notTRST	in	Test logic reset

Table 14 TAP pins

● PIO pins and alternative functions

To improve flexibility and to allow the STi5512 to fit into different set-top box application architectures, the input and output signals from some of the peripherals are not directly connected to the pins of the device. Instead they are assigned to the alternative function inputs and outputs of a PIO port bit. This scheme allows these pins to be configured as general purpose PIO if the associated peripheral input or output is not required in that particular application.

Table 17 shows the assignment of the alternative functions to the PIO bits. Parentheses ( ) in the table indicate suggested or possible pin usages as a PIO, not an alternative function connection.

Port bit	Alternative function of PIO pins				
	PIO port 0	PIO port 1	PIO port 2	PIO port 3	PIO port 4
0	ASC0TxD or Sc1DataOut	SSC0 MTSR	ASC2TxD or Sc0DataOut	SSC1 MTSR	ASC3TxD
1	ASC0TRxD or Sc1DataIn	SSC0 MRST	ASC2RxD or Sc0DataIn	SSC1 MRST	ASC3RxD
2	Sc1ClkGenExtClk	SSC0 SClk	Sc0ClkGenExtClk	SSC1 SClk	TtxtClockIn
3	Sc1Clk	PWMOut0	Sc0Clk	CaptureIn0	1284PeriphLogicH/ASC3 CTS
4	(Sc1RST)	PWMOut1	(Sc0RST)	CaptureIn1	1284HostLogicH/ASC3 RTS
5	(Sc1CmdVcc)	ASC1TxD	(Sc0CmdVcc)	CaptureIn2	Interrupt2
6	(Sc1CmdVpp) Sc1Dir	ASC1RxD	(Sc0CmdVpp) Sc2Dir	CompareOut2	Interrupt3
7	(Sc1Detect)	PWMOut2	(Sc0Detect)	1284InnotOut	TtxtData

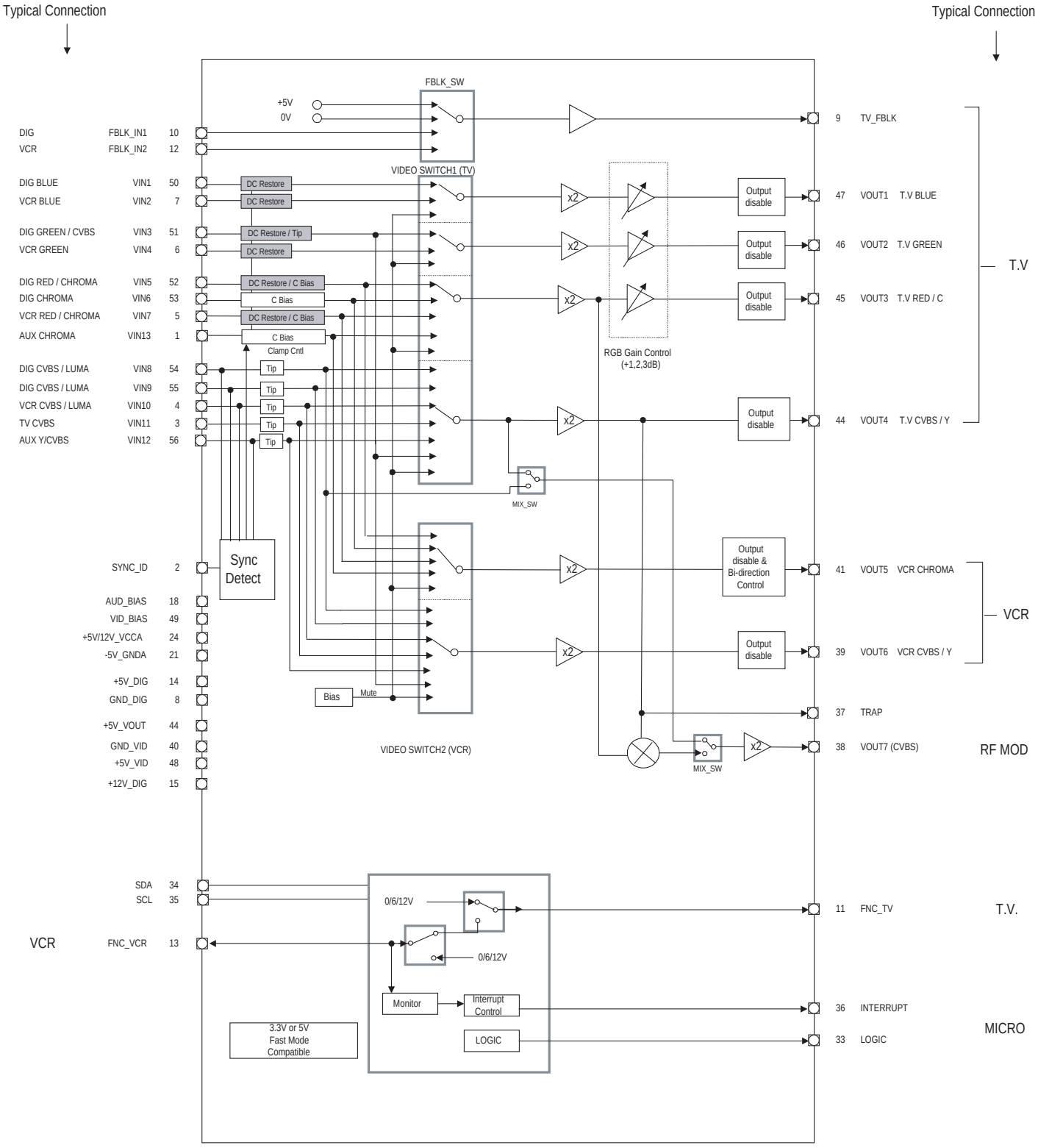
Table 15 Alternative function of PIO pins

CXA2161R (MAIN ASSY : IC4001)

- **AV Switch IC**

- **Block Diagram (1/2)**

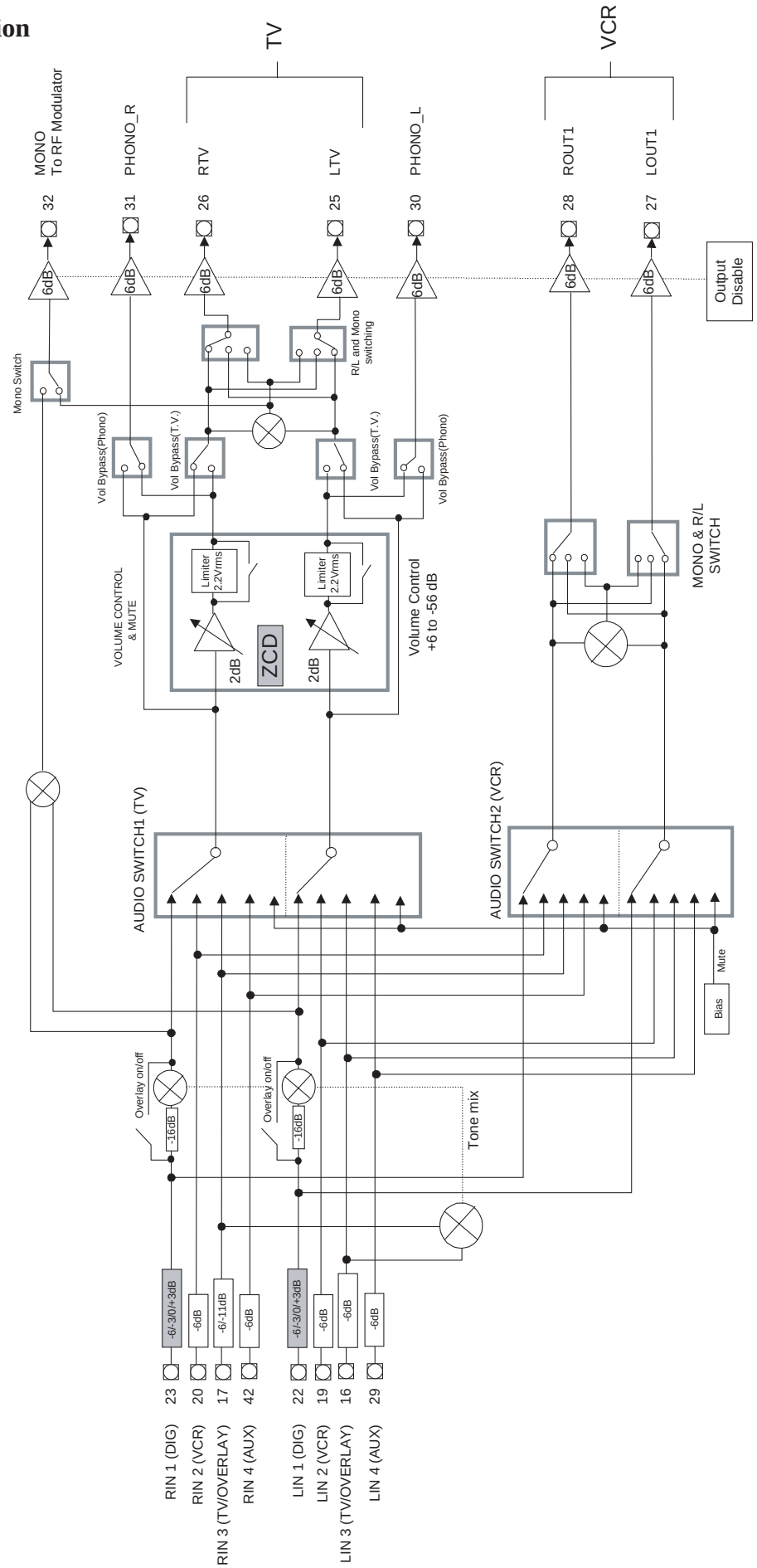
Video and Digital section



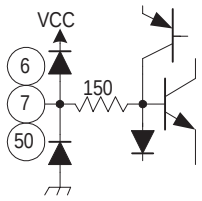
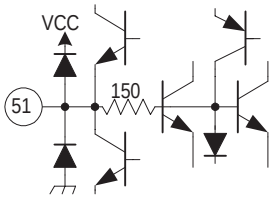
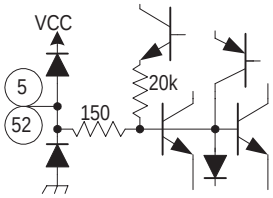
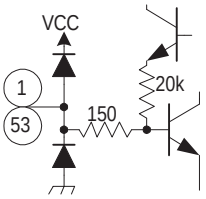
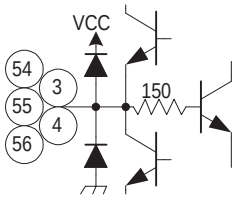
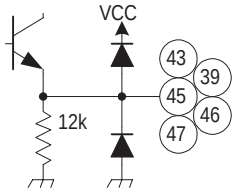
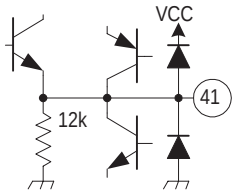
Note: All video outputs contain 75Ω drivers, except Vout7.

- **Block Diagram (2/2)**

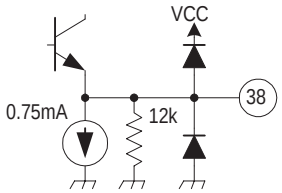
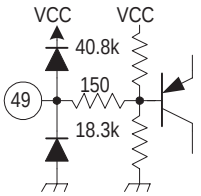
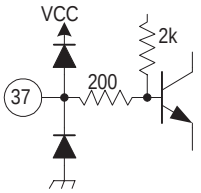
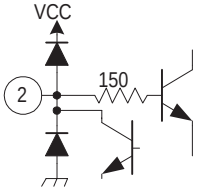
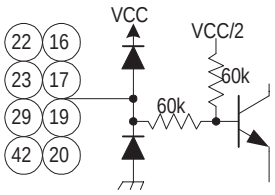
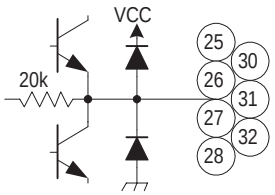
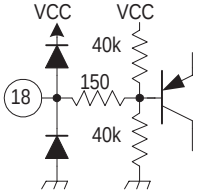
Audio section



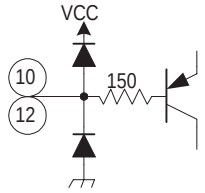
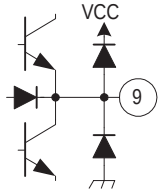
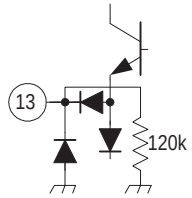
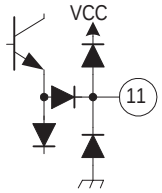
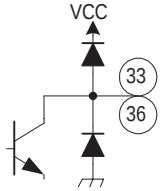
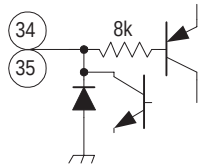
• **Pin Function (1/3)**

Pin Num	Symbol	Pin Voltage (V)	Equivalent Circuit	Description
50 7 6	VIN_1 VIN_2 VIN_4	2.4		RGB signal inputs
51	VIN_3	2.4 2.35		RGB signal input OR CVBS signal input
52 5	VIN_5 VIN_7	2.4 3.0		RGB signal inputs OR Chrominance signal inputs
53 1	VIN_6 VIN_13	3.0		Chrominance signal inputs
54 55 4 3 56	VIN_8 VIN_9 VIN_10 VIN_11 VIN_12	2.35		CVBS / Luminance signal inputs
47 46 45 43 39	VOUT_1 VOUT_2 VOUT_3 VOUT_4 VOUT_6	0.4		RGB / CVBS signal outputs
41	VOUT_5	0.4		Chrominance signal output

• **Pin Function (2/3)**

Pin Num	Symbol	Pin Voltage (V)	Equivalent Circuit	Description	
38	VOUT_7	0.4		Typically RF modulator signal output Minimum load = 20k resistive	
49	VID_BIAS	0.9		Internal reference bias for video circuits. A capacitor is connected from this pin to GND. Typically 100nF	
37	TRAP	2.3		Connects trap circuit for subcarrier	
2	SYNC_ID	2.5		Sync detect circuit time constant, resistor and capacitor connection pin	
22 23 19 20 16 17 29 42	LIN_1 RIN_1 LIN_2 RIN_2 LIN_3 RIN_3 LIN_4 RIN_4	6.0 (Single) 0.0 (Dual)		Audio signal inputs	
25 26 27 28 30 31 32	LTV RTV LOUT1 ROUT1 PHONO_L PHONO_R MONO	6.0 (Single) 0.0 (Dual)		Audio signal outputs	
18	AUD_BIAS	6.0 (Single) 0.0 (Dual)		Internal reference bias for audio circuits.	Capacitor connected to GND. (Typically 22µF) Connected directly to GND.

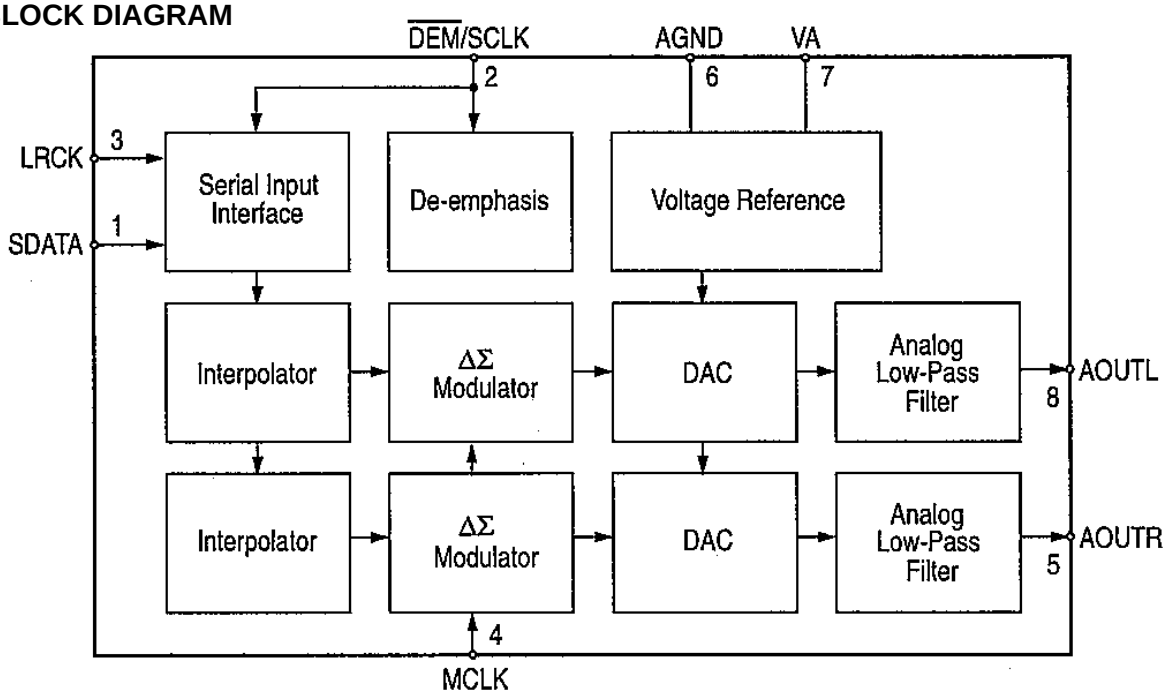
- **Pin Function (3/3)**

Pin Num	Symbol	Pin Voltage (V)	Equivalent Circuit	Description
10 12	FBLK_IN1 FBLK_IN2	-		Fast blanking signal inputs
9	TV_FBLK	-		Fast blanking signal output
13	FNC_VCR	-		SCART function pin 8 input / output to VCR
11	FNC_TV	-		SCART function pin 8 output to TV
33	LOGIC	-		Open collector logic outputs Typically connect to +5V through 10k resistor.
36	INTRUPT	-		
35	SCL	-		I^2C bus clock line
34	SDA			I^2C bus data line
14	+5V_DIG	5.0		Digital supply
44	+5V_VOUT			Video output supply
48	+5V_VID			Video supply
15	+12V_DIG	12.0		Digital supply
21	-5V_GNDA	-5.0 / 0.0		Audio supply / ground
24	+5V/12V_VCCA	5.0 / 12.0		Audio supply
8	GND_DIG	0.0		Digital ground
40	GND_VID	0.0		Video ground

■ CS4335-KS (MAIN ASSY : IC4002)

• DA Converter

● BLOCK DIAGRAM



● PIN DESCRIPTIONS

SERIAL DATA INPUT	**SDATA** 1	8 **AOUTL**	ANALOG LEFT CHANNEL OUTPUT
DE-EMPHASIS / SCLK	**DEM/SCLK** 2	7 **VA**	ANALOG POWER
LEFT / RIGHT CLOCK	**LRCK** 3	6 **AGND**	ANALOG GROUND
MASTER CLOCK	**MCLK** 4	5 **AOUTR**	ANALOG RIGHT CHANNEL OUTPUT

Power Supply Connections

VA - Analog Power, PIN 7

Analog supply. Nominally +5V.

AGND - Analog Ground, PIN 6

Analog ground reference.

Analog Outputs

AOUTL - Analog Left Cannel Output, PIN 8

Analog output for the left channel. Typically 3.5V Vpp for a full-scale input signal.

AOUTR - Analog Right Cannel Output, PIN 5

Analog output for the right channel. Typically 3.5V Vpp for a full-scale input signal.

Digital Inputs

MCLK - Master Clock Input, PIN 4

The frequency must be 256x, 384x or 512x the input sample rate in Base Rate Mode (BRM) and either 128x or 192x the input sample rate in High Rate mode (HRM).

LRCK - Left/Right Clock, PIN 3

This input determine which channel is currently being input on the Audio Serial Data Input pin, SDATA.

SDATA - Audio Serial Data Input, PIN 1

Two's complement MSB-first serial data is input on this pin. The data is clocked into the CS4335 via internal or external SCLK and the channel is determined by LRCK.

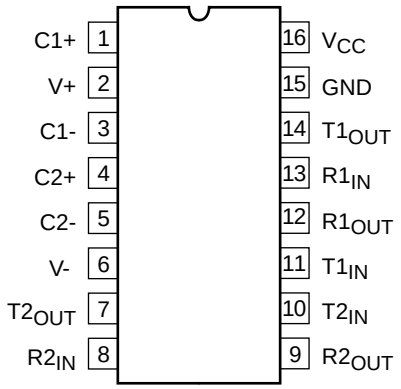
$\overline{\text{DEM}}$/SCLK - De-emphasis / External serial clock input, PIN 2

A dual-purpose input used for de-emphasis filter control or external serial clock input.

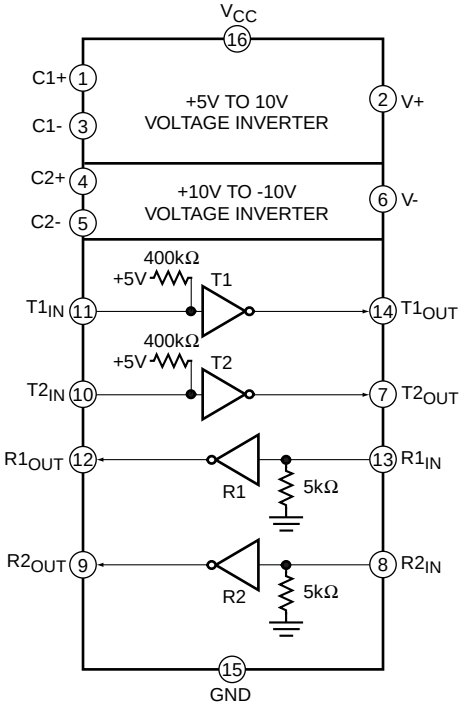
HIN202CBN (MAIN ASSY : IC5001)

- **RS232C IC**

● Pin Arrangement (Top View)



● Block Diagram



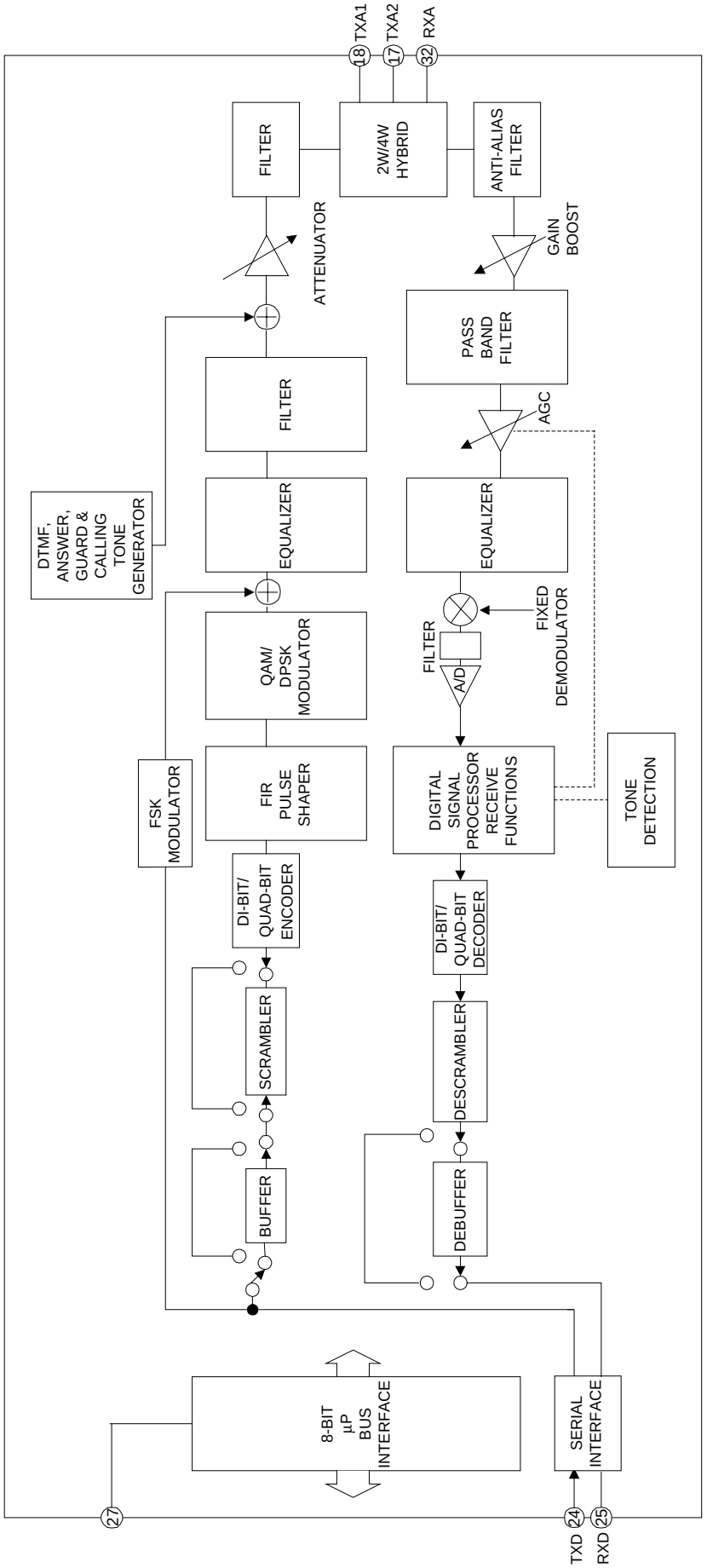
● Pin Function

No.	Name	Function
1	C1+	External capacitor (+ terminal) is connected to this lead
2	V+	Internally generated positive supply (+10V nominal)
3	C1-	External capacitor (- terminal) is connected to this lead
4	C2+	External capacitor (+ terminal) is connected to this lead
5	C2-	External capacitor (- terminal) is connected to this lead
6	V-	Internally generated negative supply (-10V nominal)
7	T2OUT	Transmitter output. This is RS-232 level (nominally ±10V)
8	R2IN	Receiver input. This input accept RS-232 input level. An internal 5kΩ pull-down resistor to GND is connected to each input.
9	R2OUT	Receiver output. This is TTL/CMOS level.
10	T2IN	Transmitter input. This lead accept TTL/CMOS level. An internal 400kΩ pull-up resistor to VCC is connected to each lead.
11	T1IN	Transmitter input. This lead accept TTL/CMOS level. An internal 400kΩ pull-up resistor to VCC is connected to each lead.
12	R1OUT	Receiver output. This is TTL/CMOS level.
13	R1IN	Receiver input. This input accept RS-232 input level. An internal 5kΩ pull-down resistor to GND is connected to each input.
14	T1OUT	Transmitter output. This is RS-232 level (nominally ±10V)
15	GND	Ground lead. Connect to 0V.
16	VCC	Power supply input 5V ±10%

■ 73K324BL-IH (MAIN ASSY : IC6005)

• **Modem IC**

● **Block Diagram**



- **Pin Function (1/3)**

POWER

NAME	PIN	TYPE	DESCRIPTION
GND	1	I	System ground
VDD	16	I	Power supply input, 5 V ±10% (73K324BL). Bypass with 0.1 and 22 μF capacitors to GND.
VREF	31	O	An internally generated reference voltage. Bypass with 0.1 μF capacitor to ground.
ISET	28	I	Chip current reference. Sets bias current for op-amps. The chip current is set by connecting this pin to VDD through a 2 MΩ resistor. ISET should be bypassed to GND with a 0.1 μF capacitor.

PARALLEL MICROPROCESSOR CONTROL INTERFACE MODE

ALE	13	I	ADDRESS LATCH ENABLE: The falling edge of ALE latches the address on AD0-AD2 and the chip select on &6 .
AD0-AD7	5-12	I/O	ADDRESS/DATA BUS: These bi-directional tri-state multiplexed lines carry information to and from the internal registers.
$\overline{CS}$	23	I	CHIP SELECT: A low on this pin during the falling edge of ALE allows a read cycle or a write cycle to occur. AD0-AD7 will not be driven and no registers will be written if $\overline{CS}$ (latched) is not active. The state of $\overline{CS}$ is latched on the falling edge of ALE.
CLK	2	O	OUTPUT CLOCK: This pin is selectable under processor control to be either the crystal frequency (for use as a processor clock) or 16 times the data rate for use as a baud rate clock in DPSK modes only. The pin defaults to the crystal frequency on reset.
$\overline{INT}$	20	O	INTERRUPT: This open drain output signal is used to inform the processor that a detect flag has occurred. The processor must then read the Detect Register to determine which detect triggered the interrupt. $\overline{INT}$ will stay low until the processor reads the detect register or does a full reset.
$\overline{RD}$	15	I	READ: A low requests a read of the 73K324BL internal registers. Data can not be output unless both $\overline{RD}$ and the latched $\overline{CS}$ are active or low.
RESET	30	I	RESET: An active high signal on this pin will put the chip into an inactive state. All Control Register bits (CR0, CR1, tone) will be reset. The output of the CLK pin will be set to the crystal frequency. An internal pull-down resistor permits power-on-reset using a capacitor to VDD.

- **Pin Function (2/3)**

PARALLEL MICROPROCESSOR INTERFACE (continued)

NAME	PIN	TYPE	DESCRIPTION
$\overline{WR}$	14	I	WRITE: A low on this informs the 73K324BL that data is available on AD0-AD7 for writing into an internal register. Data is latched on the rising edge of $\overline{WR}$. No data is written unless both $\overline{WR}$ and the latched $\overline{CS}$ are low.

SERIAL MICROPROCESSOR CONTROL INTERFACE MODE

NAME	PIN	TYPE	DESCRIPTION
AD0-AD2	5-7	I	REGISTER ADDRESS SELECTION: These lines carry register addresses and should be valid during any read or write operation.
DATA (AD7)	12	I/O	SERIAL CONTROL DATA: Data for a read/write operation is clocked in or out on the falling edge of the EXCLK pin. The direction of data flow is controlled by the $\overline{RD}$ pin. $\overline{RD}$ low outputs data. $\overline{RD}$ high inputs data.
$\overline{RD}$	15	I	READ: A low on this input informs the 73K324BL that data or status information is being read by the processor. The falling edge of the $\overline{RD}$ signal will initiate a read from the addressed register. The $\overline{RD}$ signal must continue for eight falling edges of EXCLK in order to read all eight bits of the referenced register. Read data is provided LSB first. Data will not be output unless the $\overline{RD}$ signal is active.
$\overline{WR}$	14	I	WRITE: A low on this input informs the 73K324BL that data or status information has been shifted in through the DATA pin and is available for writing to an internal register. The normal procedure for a write is to shift in data LSB first on the DATA pin for eight consecutive falling edges of EXCLK and then to pulse $\overline{WR}$ low. Data is written on the rising edge of $\overline{WR}$.

NOTE: The serial control mode is provided by tying ALE high and $\overline{CS}$ low. In this configuration AD7 becomes DATA and AD0, AD1 and AD2 become the register address.

- **Pin Function (3/3)**

DTE USER

NAME	PIN	TYPE	DESCRIPTION
EXCLK	22	I	EXTERNAL CLOCK: This signal is used in synchronous transmission when the external timing option has been selected. In the external timing mode the rising edge of EXCLK is used to strobe synchronous DPSK transmit data applied to on the TXD pin. Also used for serial control interface.
RXCLK	26	O	RECEIVE CLOCK: The falling edge of this clock output is coincident with the transitions in the serial received data output. The rising edge of RXCLK can be used to latch the valid output data. RXCLK will be valid as long as a carrier is present.
RXD	25	O	RECEIVED DATA OUTPUT: Serial receive data is available on this pin. The data is always valid on the rising edge of RXCLK when in synchronous mode. RXD will output constant marks if no carrier is detected.
TXCLK	21	O	TRANSMIT CLOCK: This signal is used in synchronous transmission to latch serial input data on the TXD pin. Data must be provided so that valid data is available on the rising edge of the TXCLK. The transmit clock is derived from different sources depending upon the synchronization mode selection. In internal mode the clock is generated internally. In external mode TXCLK is phase locked to the EXCLK pin. In slave mode TXCLK is phase locked to the RXCLK pin. TXCLK is always active.
TXD	24	I	TRANSMIT DATA INPUT: Serial data for transmission is applied on this pin. In synchronous modes, the data must be valid on the rising edge of the TXCLK clock. In asynchronous modes (1200/600 bps or 300/1200 baud) no clocking is necessary. DPSK data must be 1200/600 bps +1%, -2.5% or +2.3%, -2.5 % in extended over speed mode.

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ANALOG INTERFACE AND OSCILLATOR

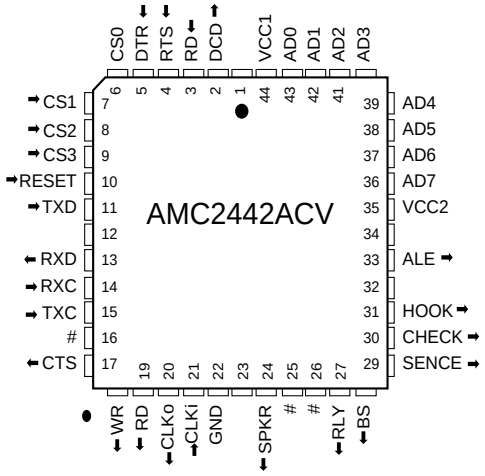
NAME	PIN	TYPE	DESCRIPTION
RXA	32	I	Received modulated analog signal input from the telephone line interface.
TXA1 / TXA 2	18 / 17	O	(differential) Transmit Analog. These pins provide the analog output signals to be transmitted to the telephone line. The drivers will differentially drive the impedance of the line transformer and the line matching resistor. An external hybrid can also be built using TXA1 as a single ended transmit signal.
XTL1 / XTL2	3 / 4	I	These pins are for the internal crystal oscillator requiring a 11.0592 MHz parallel mode crystal. Load capacitors should be connected from XTL1 and XTL2 to ground. XTL2 can also be driven from an external clock.
$\overline{OH}$	27	O	OFF-HOOK RELAY DRIVER: This signal is an open drain output capable of sinking 40 mA and is used for controlling a relay. The output is the complement of the OH register bit in the ID Register.

AMC2442ACV(0.84) (MAIN ASSY : IC6006)

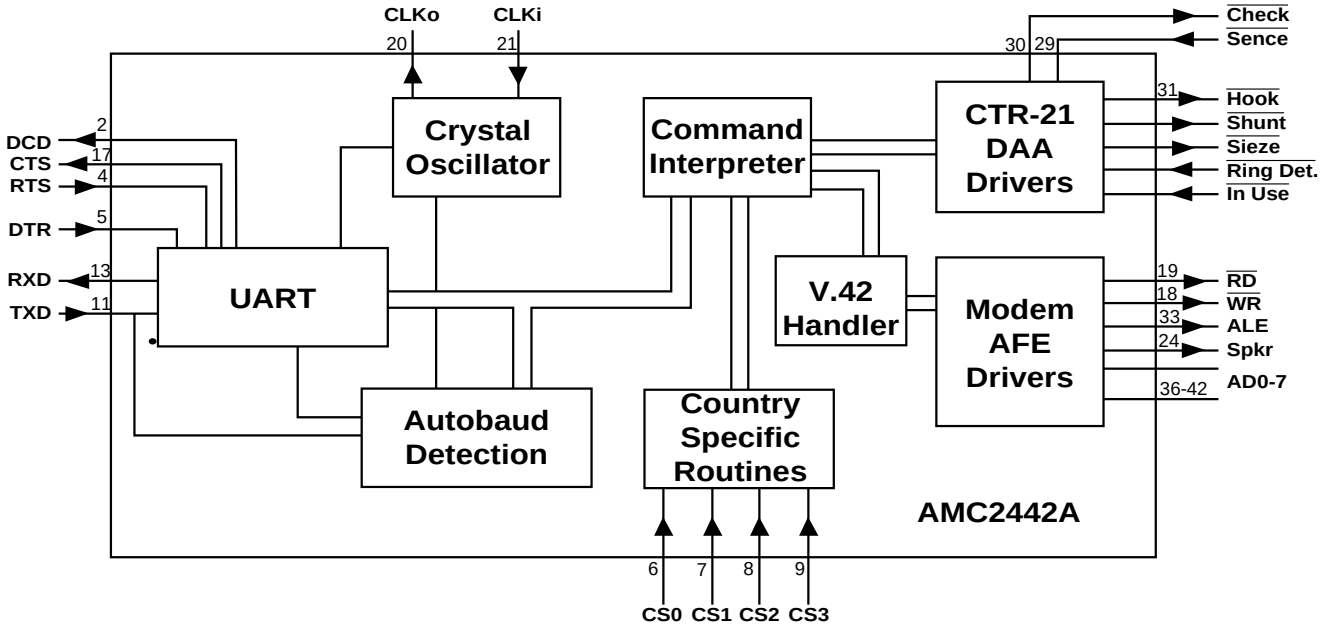
- **Modem Controller**

● **Pinouts / Block Diagram**

Pinouts



BLOCK DIAGRAM



● Pin Function

PIN NUMBER	Pin Name	I/O TYPE	Description
2	DCD	Output	DTE Data Carrier Detect output signal. Indicates modem has detected carrier.
3	RING	Input	Ring detector input. This pin assumes that a half wave opto coupler is used in the telephone line DAA circuit in the frequency detection algorithm.
4	RTS	Input	DTE Ready To Send input signal. Used for hardware flow control.
5	DTR	Input	DTE Data Terminal Ready input signal. Used to enable modem device
6	CS0	Intput	Country Selection bit 0 (Internal pull up)
7	CS1	Input	Country Selection bit 1 (Internal pull up)
8	CS2	Input	Country Selection bit 2 (Internal pull up)
9	CS3	Input	Country Selection bit 3 (Internal pull up)
10	RESET	Input	Reset signal to the AMC2442A Controller. Active High.
11	TXD	Input	DTE Transmit Data Pin. All data communication from the DTE connects via this pin.
13	RXD	Output	DTE Receive Data Pin. All data communication to the DTE connects via this pin.
14	RXC	Input	Receiver Clock Input from AFE. Used in PSK, QAM and synchronous data mode.
15	TXC	Input	Transmitter Clock Input from AFE. Used in PSK, QAM and synchronous data mode.
16	Free	I/O	DO NOT CONNECT
17	CTS	Output	DTE Clear To Send output signal. Used for hardware flow control.
18	WR	Output	Write signal to AFE. Goes active low whenever the SMC wishes to write to the AFE
19	RD	Output	Read signal to AFE. Goes active low whenever the SMC wishes to read from the AFE
20	CLKo	Output	Buffered Clock output signal. Also used as a crystal drive signal when required.
21	CLKi	Input	Clock input signal. The SMC requires an 11.0592MHz signal on this pin.
22	GND	Power	Controller Ground connection
24	SPKR	Output	Speaker Enable drive
25	Free	I/O	DO NOT CONNECT
26	Free	I/O	DO NOT CONNECT
27	RLY	Output	DAA Line Seize relay control. Used if DPCO relay is used to share the telephone with a standard telephone instrument.
28	BS	Output	DAA Bell Shunt control. Used during LD dialling to provide a low impedance loop.
29	SENSE	Input	Line-In-Use detection input.
30	CHECK	Output	Line-In-Use circuit drive pin.
31	HOOK	Output	DAA Hook switch control. Delayed from Seize to allow for a low cost opto coupler.
32	NC	I/O	DO NOT CONNECT
33	LATCH	Output	ALE signal to AFE. Goes active high to latch an address into the AFE
35	VCC2	Power	Auxiliary power supply pin.
36->43	AD7->AD0	I/O	Multiplex Address / Data bus connections to AFE.
44	VCC1	Power	Main power supply pin.
1	NC	I/O	DO NOT CONNECT
12	NC	I/O	DO NOT CONNECT
23	NC	I/O	DO NOT CONNECT
34	NC	I/O	DO NOT CONNECT

■ PE5181A (MAIN ASSY : IC7001)

• **Sub CPU**

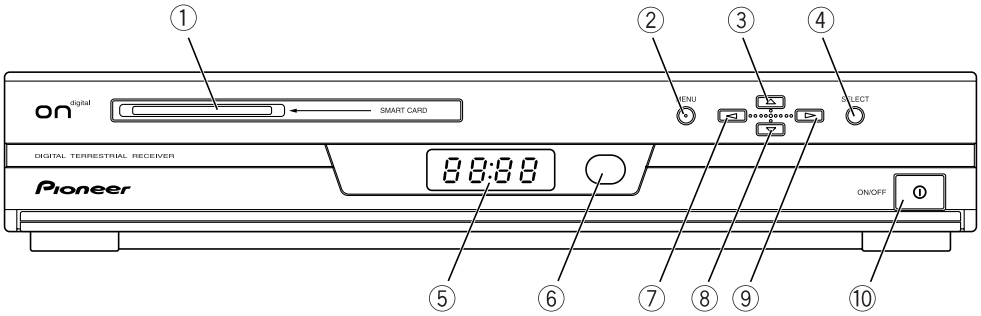
● **Pin Function**

No.	Mark	Pin Name	I/O	Active	Pin Function
1	P50	LED10	O	Low	Front LED, seg
2	P51	LED11	O	Low	Front LED, seg
3	P52	LED12	O	Low	Front LED, seg
4	P53	LED13	O	Low	Front LED, seg
5	P54	LED14	O	Low	Front LED, seg
6	P55	LED15	O	Low	Front LED, seg
7	P56	LED16	O	Low	Front LED, seg
8	P57	LED17	O	Low	Front LED, seg
11	P30	IRQ_TEIDEN	O	Low	Power failure interruption (L output only at power failure)
12	P31	IRQ_KEY	O	Low	Remote controller / key interruption
13	SDA0	I2C_SDA	O		I2C_SDA Output
14	SCL0	I2C_SCL	I		I2C_SCL Input
15	P34	×	O		
16	P35	×	O		
17	P36	×	O		
18	P20	×	O		
19	P21	×	O		
20	P22	×	O		
21	P23	×	O		
22	P24	×	O		
23	P25	SUB_MUTE	O	Low	Power_off Mute
26	P17	TEST	I	Low	For production line
27	P16	RC_MM	I	Any	RC_MM Selection (H : Disabel, L : Enable)
28	P15	pioneer/philips	I	Any	Remote control code selection (H : Philips, L : Pioneer)
29	P14	XHALT	I	Low	Power failure process completion flag (L : Complete, H : Normaly)
30	P13	×	I		For AGC Reading
31	P12	KEY02, MENU	I	Low	Front key input
32	P11	KEY01, OK	I	Low	Front key input
33	P10	KEY00, ←	I	Low	Front key input
43	INTP0	REM	I	High	Remote control input
44	INTP1	AC_CLK	I	Toggle	Power failuer detection clock (Both edge detectin)
45	P02	LNB_POW0	O	Any	LNB inernal / external (H : internal, L : external)
46	P03	LNB_POW1	O	Any	LNB 18V / 13V (H : 18V, L : 13V)
47	TI00	REM	I	High	Remote control input
48	P71	KEY, ↑	I		Front key input
49	P72	×	O		
50	P73	XSTBY	O	Low	Stand-by signal (H output at full power)
51	P74	KEY, ↓	I		Front key input
52	P75	KEY, →	I		Front key input
53	P64	XRESET_OMEGA	O	Low	STi5512 Reset
54	P65	RESET_CHDEC	O/I	High	Link IC Reset
55	P66	×	O		
56	P67	×	O		
57	P40	×	O		
58	P41	×	O		
59	P42	×	O		
60	P43	×	O		
61	P44	LED03	O	Low	Front LED, dig
62	P45	LED02	O	Low	Front LED, dig
63	P46	LED01	O	Low	Front LED, dig
64	P47	LED00	O	Low	Front LED, dig

8. PANEL FACILITIES AND SPECIFICATIONS

8.1 PANEL FACILITIES

■ Front View (Front Panel)



① **Smartcard slot**

② **MENU button:**
Displays and closes Main Menu

③ **▲ :** Moves the highlight towards the top of the menu

④ **SELECT button:**
Displays the channel list while in the TV mode.
Confirms the menu selections

⑤ **4-digit LED front indicator light**

⑥ **Infrared sensor**

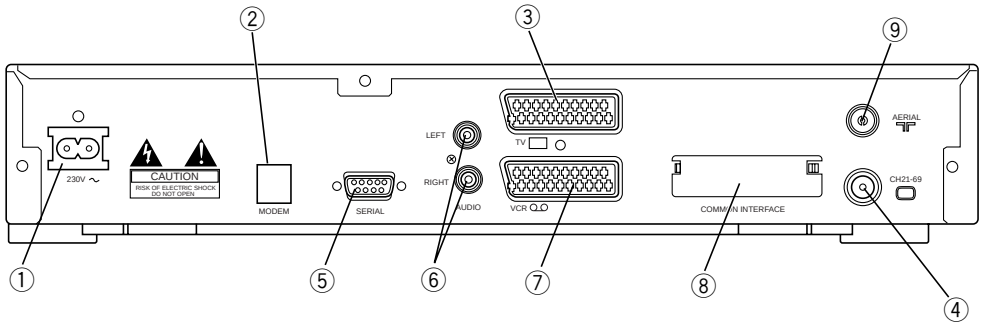
⑦ **◄ :** Adjusts menu option settings

⑧ **▼ :** Moves the highlight towards the bottom of the menu

⑨ **► :** Adjusts menu option settings

⑩ **Main Switch button**

■ Rear View (Back Panel)



① **230 V, 50 Hz main lead socket (excessive voltage)**

② **RJ11 telephone line connector (TNV*)**
NOTE:
Required for pay-per-view and other interactive applications.

③ **SCART** socket for TV set (SELV***)**

④ **UHF**** aerial output for TV set (SELV***)**

⑤ **RS-232C***** serial port socket (SELV***)**
NOTE:
Not required for current application but necessary for the future services.

⑥ **Audio-sync outputs for stereo system (SELV***)**

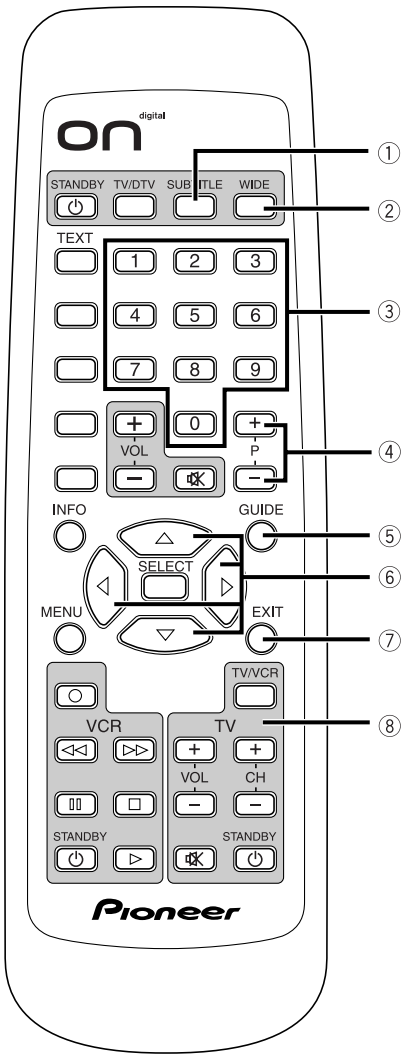
⑦ **SCART** socket for VCR (SELV***)**

⑧ **COMMON INTERFACE (SELV***)**
NOTE:
For future use.

⑨ **UHF**** antenna input (SELV***)**

** TNV*	*:Telecommunication Network Voltage*
*** SCART*	*:Euroconnector*
**** SELV*	*:Safety Extra Low Voltage*
***** UHF*	*:Ultra High Frequency*
****** RS-232C*	*:Ready to connect multimedia product.*

■ Remote Control Unit (1/2)



① **SUBTITLE button**
Press this button to display subtitles on the screen.

② **WIDE button**
Press this button to switch between wide-screen and cropped movies.

③ **0 - 9 (Numeral) button**
Press these buttons to directly select a channel or to make on-screen menu selections.

④ **P (PROGRAM) (+), (-) button**
These buttons are used for channel selection.

⑤ **GUIDE button**
Not currently used.

⑥ **▲, ▼, ◄, ► button**
- Up/Down buttons: These buttons are used for menu and programme selections when the channel list is displayed.
- Left/Right buttons: These buttons are used for menu confirmation.

⑦ **EXIT button**
This button is used to cancel the menu screen settings.

⑧ Refer to "Setting TV Codes" on the instruction manual.

Function of receiver front panel buttons:
- *In Standby mode: Pressing any button wakes up the receiver from standby.*
- *In Normal mode: The buttons have the same functions as the corresponding remote control buttons. (See below.)*
  ◄/►=LEFT/RIGHT; ▲/ ▼=UP/DOWN

■ Remote Control Unit (2/2)

⑨ **TV/DTV button**
This button is used to switch between digital and analogue broadcasting.
NOTE:
This button is operative only when your ONdigital box and TV are connected by a scart lead.

⑩ **STANDBY button**
Switches ONdigital box in and out of standby.
NOTE:
The receiver will not operate unless the main power switch is turned on first.

⑪ **TEXT button**
Pressing this button selects Text Mode.

⑫ **RED, GREEN, YELLOW, BLUE button**
These buttons are used for Text Mode and menu screen operation.

⑬ **VOL (+), (-) button**
These buttons can be used to adjust volume.

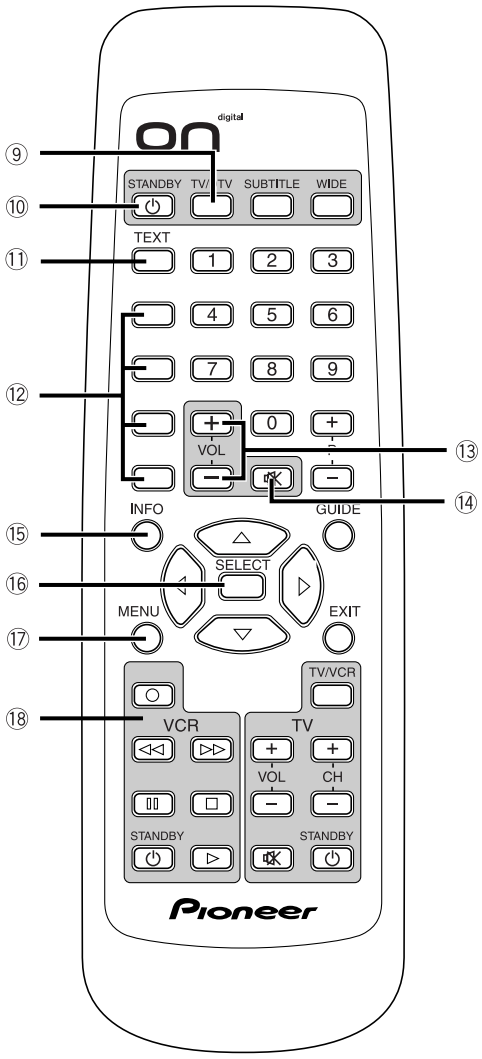
⑭ **MUTE button**
Is used to mute the sound. Pressing the button again turns the sound on again at the volume it was at when muted.

⑮ **INFO button**
Pressing this button displays the on-screen tv guide.

⑯ **SELECT button**
- When watching a programme, this button is used to display the channel list.
- When the channel list is displayed, this button is used to select a programme.
- When the menu screen is displayed, this button is used to confirm the selected menu item.

⑰ **MENU button**
Pressing this button displays the menu screen.

⑱ Refer to "Setting VCR Codes" on the instruction manual.



8.2 SPECIFICATIONS

System capabilities
- DVB compliant MPEG-2 reception of broadcasts up to Main Profile @ Main Level

Video decoding
- DVB compliant MPEG-2 reception of broadcasts up to MP @ ML
- Video bit rate :up to 15 Mbit/sec
- Video format :4:3 and 16:9
- Resolution :up to 720 by 576 pixels

Audio decoding
- MPEG layer I/II (excluding multichannel management from one bit stream)

Operation/Features
- Automatic program loading via scanning installation
- Free to air reception
- DVB subtitles
- Program parental lock with PIN code
- Audio mode : single channel, dual channel, stereo, joint stereo
- Volume control
- Full remote controlled
- Menu controlled operation using on-screen display
- Menu controlled installation using on-screen display
- 8 events over one year VCR timer
- Automatic VCR play back
- Receiver compatible with ONdigital services
- Electronic programme guide for ONdigital bouquet services
- Main switch
- Multibrand TV and VCR remote control

Reception-Demodulation
- Demodulation according DVB-T
  Type COFDM 2K
  Mode All mode
  Non hierarchical

Descrambling

Embedded Mediaguard and PCMCIA interface for the Common Interface CA-module (DVB standard).

NOTE:
subscription is required for the reception of ONdigital scrambled services

Connections
- RF input (for aerial) connector: female IEC 169-2
  Input frequency range (MHz): 471-855 (CH21 to 69)
- RF output (to TV) connector: male IEC 169-2
  Loopthrough frequency range (MHz) 471-855 (CH21 to 69)
  Redemodulated output PAL I
  CH21-69 range
  Preset CH38
- TV SCART
  Output: CVBS, Controlled audio L/R, RGB, Slow blanking, Fast blanking
- VCR SCART
  Input: CVBS, Slow blanking, Audio L/R
  Output: CVBS, Audio L/R
- Audio CINCH
  Output: Controlled audio L/R
- Serial interface: RS 232/DB 9 female
- Integrated modem telephone line interface : RJ-11
- Common interface for type II or III module

Return path
- Integrated Telephone modem
- Type V22 bis
- Error correction V42
- Dialling mode DTMF and pulse

Accessories
- Remote control
- SCART cable
- Instruction book
- ONdigital Envelope
- Telephone cord with plugs (10 m)
- Batteries : 2 x 1.5V type AA/R06/UM-3
- UHF coaxial lead
- Mains cord

Miscellaneous
- Operating Temperature : +5 ˚C to 45 ˚C
- Mains : 230 V +/-10%, 50 Hz
- Power consumption (W) 15 max
- Standby consumption (W) 5.5 max
- Weight (kg) 2.2 (with no packaging or accessories)
- Dimensions (w x h x d mm) 380 x 71 x 259

Specifications and design are subject to possible modifications without notice due to improvements.